

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
DDRIII DIMMA1&DDRIII DIMMB1	7,8
LYNX-PCI/E/DMI/USB/CLK	9
LYNX-SATA/HOST/FAN/GPIO/VGA	10
LYNX-SMB/LPC/AUDIO/RTC/RST	11
LYNX-POWER PIN,GND/LYNX STRAPS	12,13 ,14
PCIE1(X1) & PCIE2(X16) Slots	15
ASM1083 PCIE to PCI bridge	16
PCI SLOT X1	17
SIO-NUVOTON NCT6779D	18
ALC892/887	19
LAN RTL8111G/8106E	20
SATA /USB3.0 Connector	21
USB3.0 Renes UPD720202 2PORT	22
USB2.0 Connector	23
VGA,DVI , HDMI ,	24-26
FAN	27
ACPI Controller UPI	28
CPU Power - ISL95812,CPU Power - MOS	29
DDR Power -UP1513 1-Phase	30
PCH Power - OP+MOS	31
PCH Power - ME Power	32
FAN	33
ATX F_Panel/EMI/TPM/LPT	34
XDP CPU & COM PORT	34
Manual Parts	34

MS-7846

mATX
Ver: 3.0

Intel Sharkbay plamform H81 COLAY B85 H87

CPU: *INTEL-Haswell LGA1150*

System Chipset: *H81,B85,H87*

Memory: *DDRIII (1333/1666MHz) * 2 (Dual Channel)*

PWM: *VRD12 - ISL95812*

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-realtek8111G

SIO:NUVOTON 6779D

SPI ROM: 64 MB & 128MB

Other:

*VGA*1*

*SATA gen2*2*

*SATA gen3*4*

*FRONT USB2.0 *4*

*FRONT USB3.0 *2*

*REAL USB2.0 *2*

*REAL USB3.0 *2*

*PS2*1*

*FRONT COM PORT*1*

*Front PRINT PORT*1*

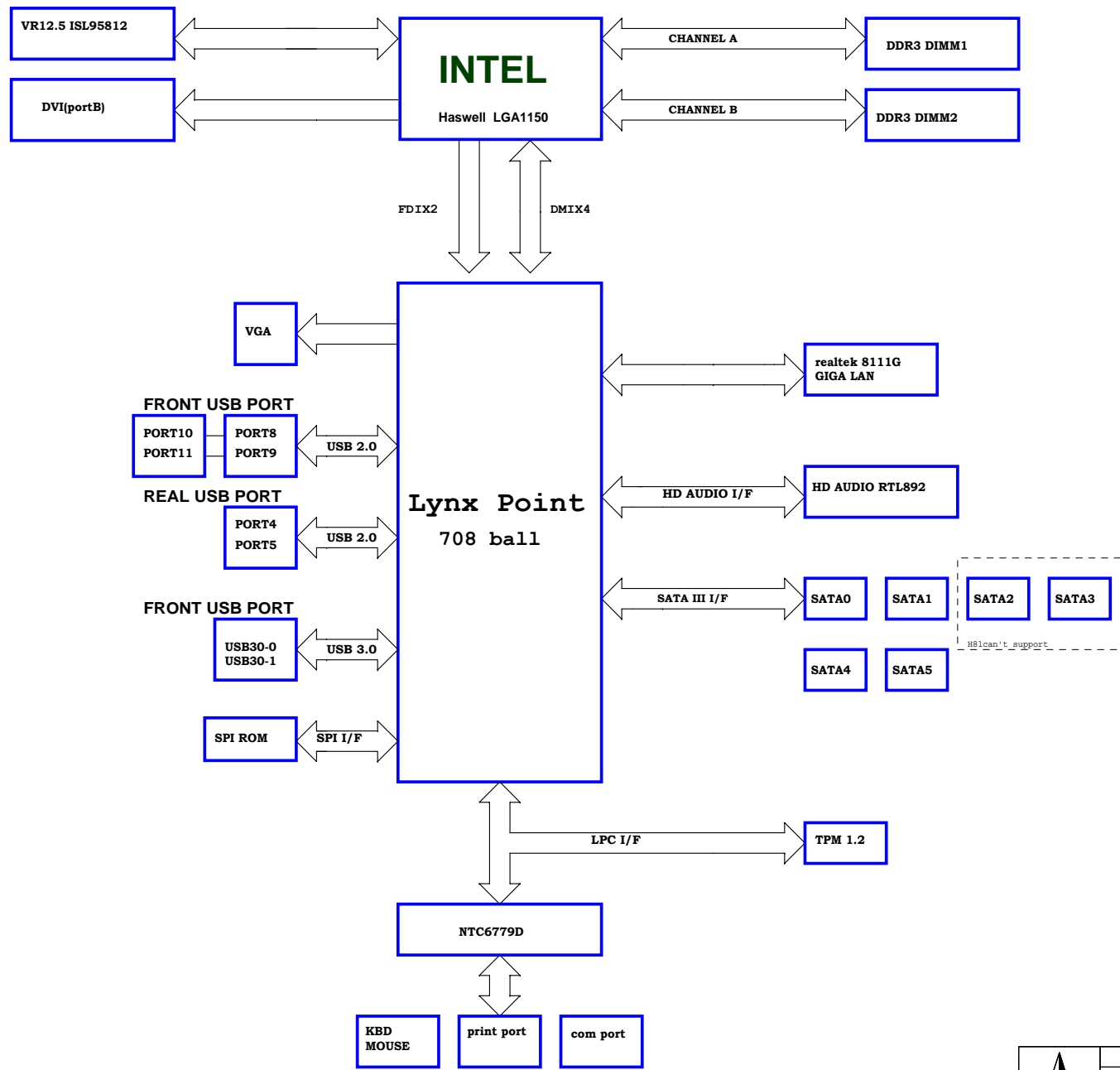
Expansion Slots:

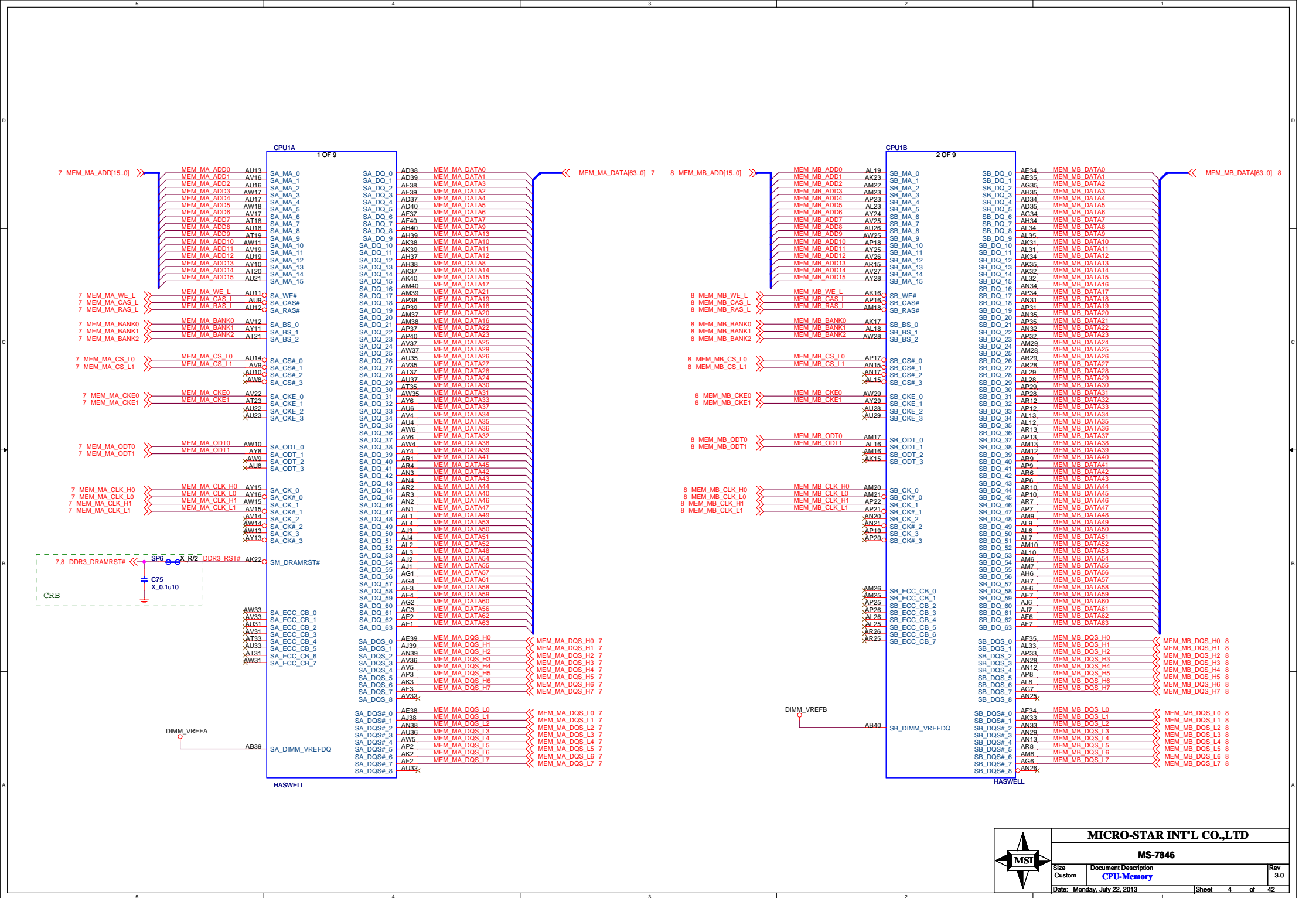
*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

*PCI Slot * 1*

MS-7846 Block Diagram





GND

GND

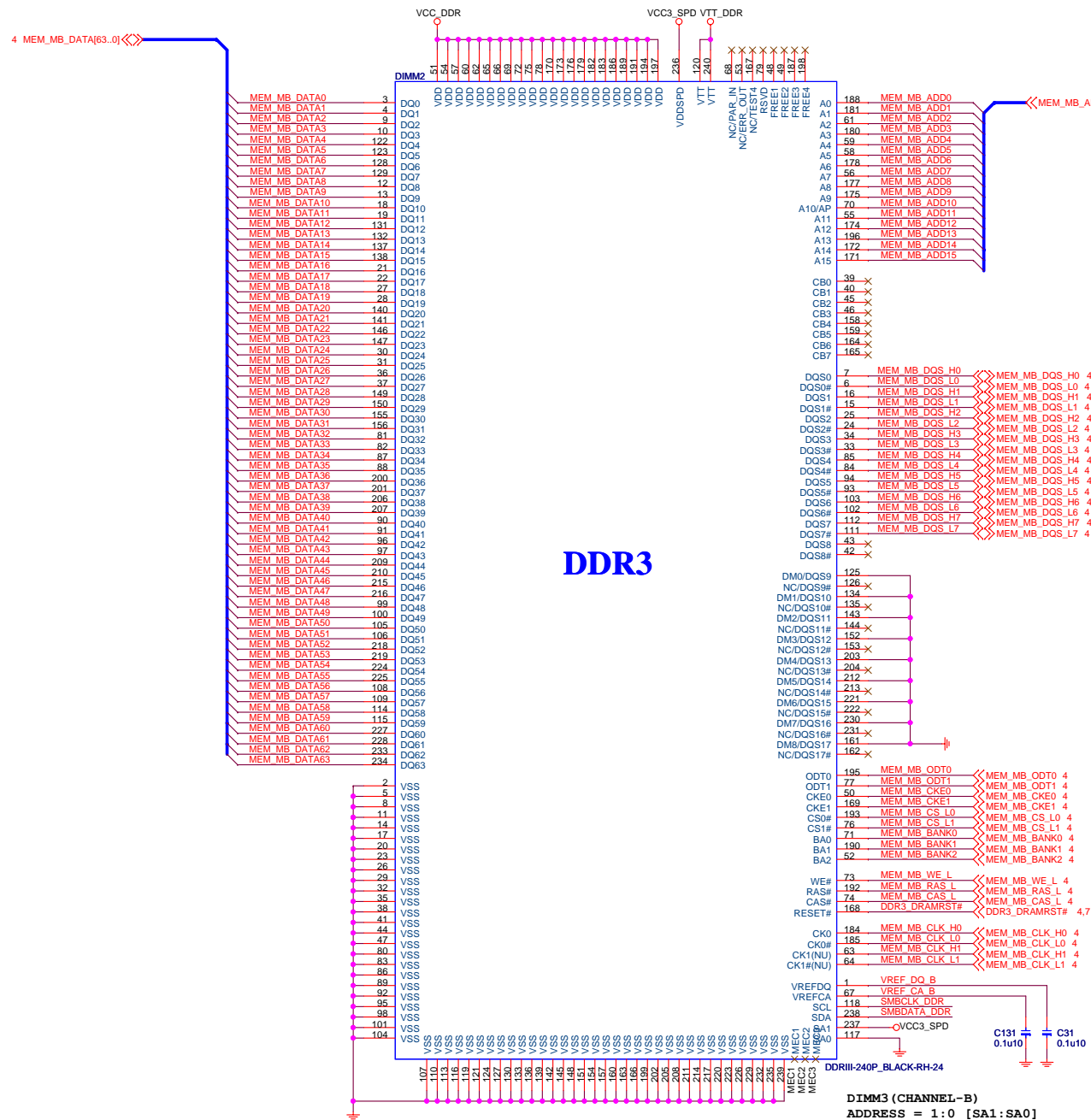


MICRO-STAR INT'L CO.,LTD

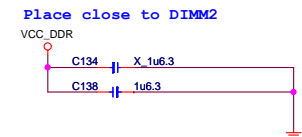
MS-7846

Size	Document Description	Rev
Custom	CPU-GND	3.0
Date: Monday, July 22, 2013		Sheet 6 of 42

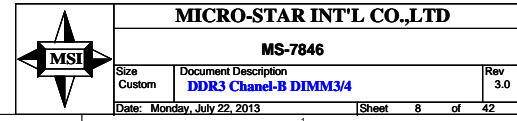
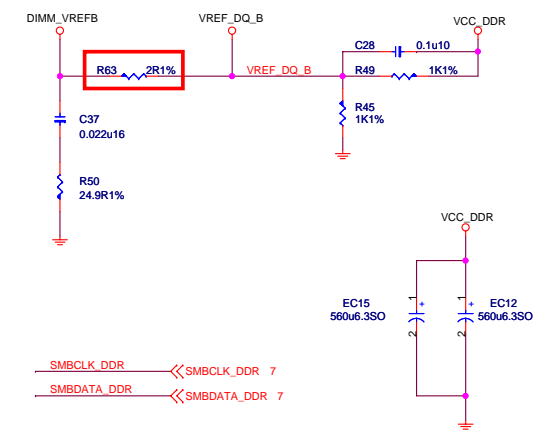
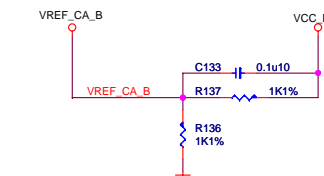
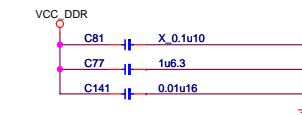
DDRIII DIMM_B0



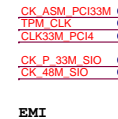
DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]



Place close to DIMM2




```
pcie port7,8 NA
```

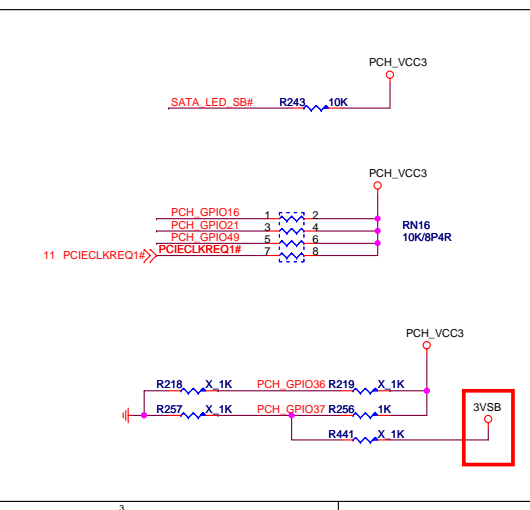
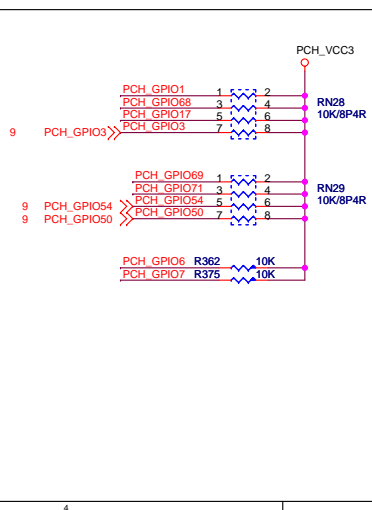
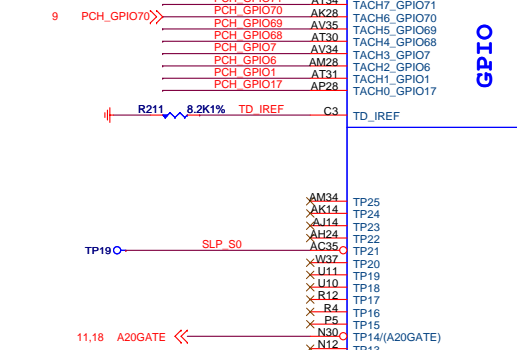


MS-7846

Size Custom	Document Description PPT PCIE/DMI/USB/CLK	Rev 3.0
Date: Monday, July 22, 2013	Sheet 9 of 42	

R439 for H81 R438 for H87 B85

35 PCH_MEPWROK >> R438 X_OR
5,11,14,18 CHIP_PWGD >> R439 OR ME_PWGD



Enable VGA (CTRLCLK/DATA Pull High)

PCH_VCC3

HDMI_DDPD_CTRLCLK R471 X 2.2K/4
HDMI_DDPD_CTRLDATA R472 X 2.2K/4

DVI_DDPD_CTRLCLK R474 2.2K/4
DVI_DDPD_CTRLDATA R473 2.2K/4

Close to PCH within 250mils.

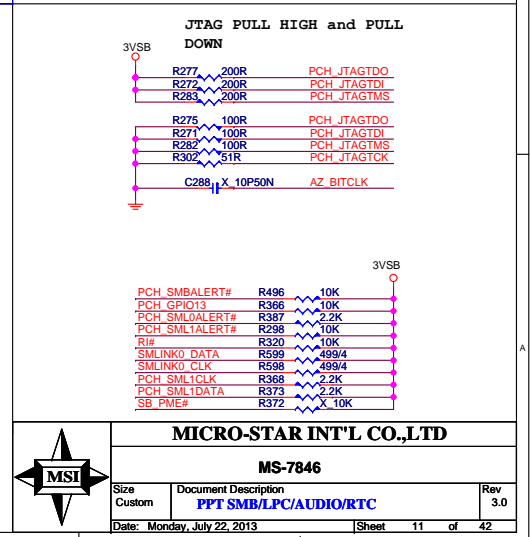
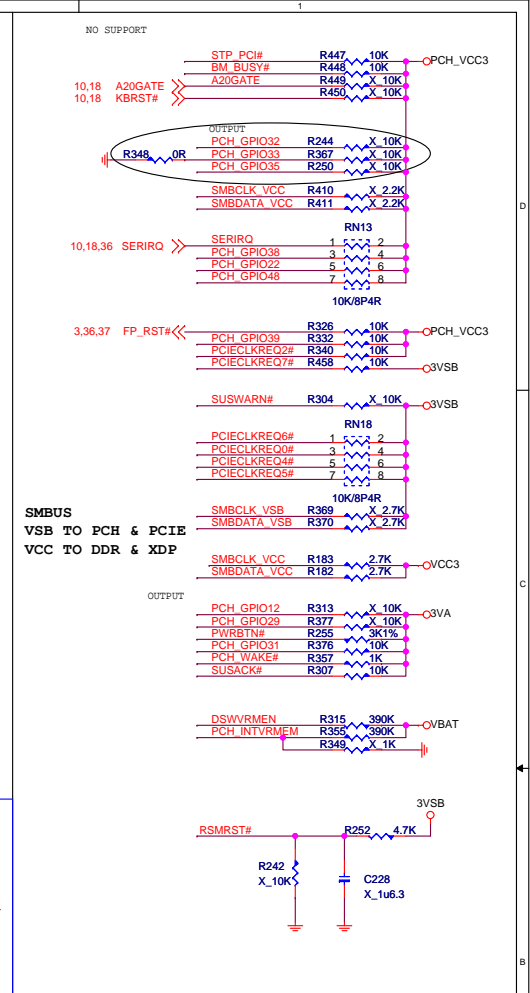
VGA_R R284 150R1%
VGA_G R295 150R1%
VGA_B R278 150R1%

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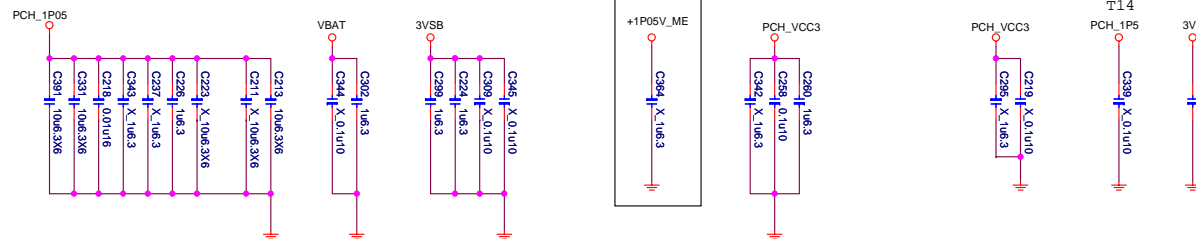
MS-7846

Size Custom Document Description **PPT SATA/HOST/FAN/GPIO/VGA** Rev 3.0

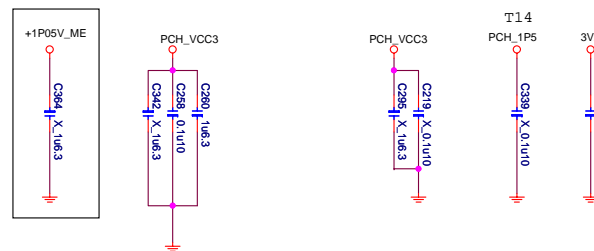
Date: Monday, July 22, 2013 Sheet 10 of 42



PCH_1P05 5.747A



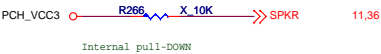
PCH_VCC3 HAVE SEQUENCING



MS-7846

Size Custom	Document Description LYNX -POWER PIN	Rev 3.0
Date: Monday, July 22, 2013		Sheet 12 of 42

PCH Straps

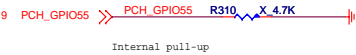


SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

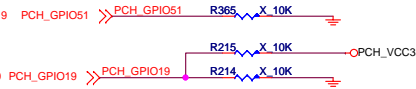


GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GF/GPIO19, GPIO51

Default (SPI):

Left both SATA1GF/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

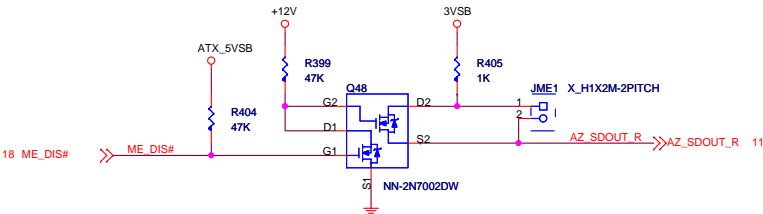
Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.

Connect to ground with 1k Ohm pull-down resistor.



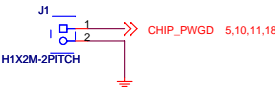
HDA_SDO

Default:

Do not pull high.

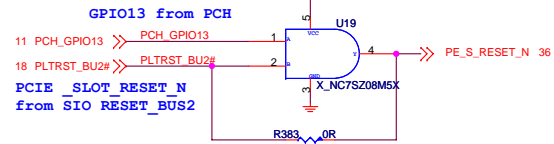
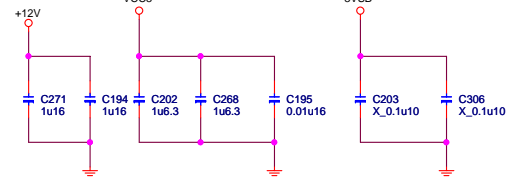
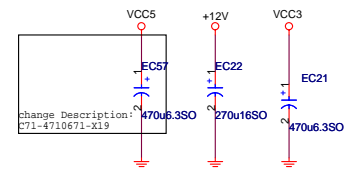
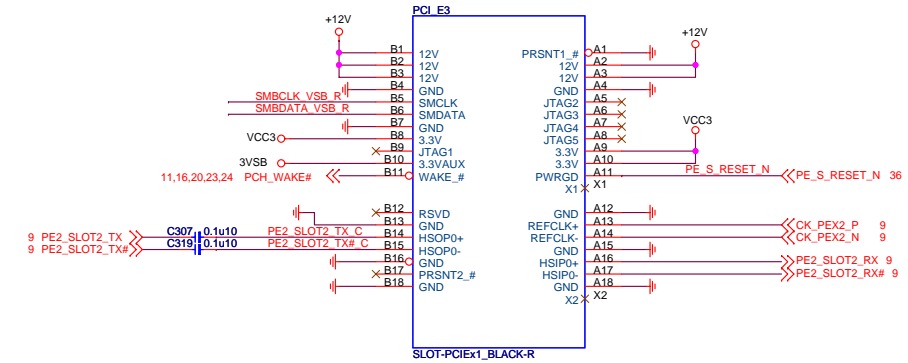
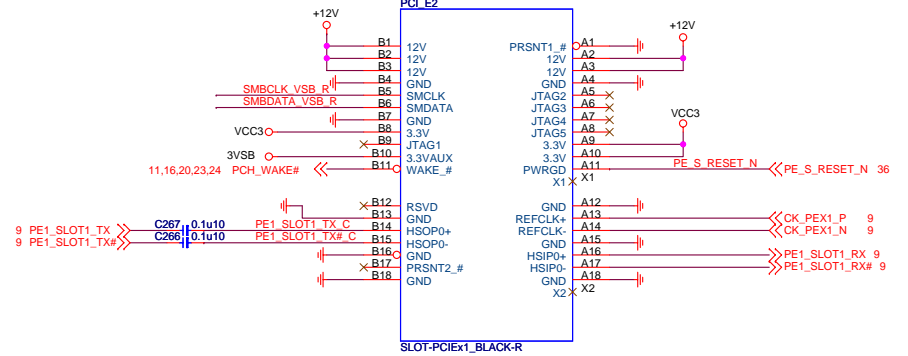
Disable ME in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

For test cpu voltage



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MS-7846		
Size Custom	Document Description PPT STRAPS	Rev 3.0
Date: Monday, July 22, 2013		Sheet 14 of 42

11 SMBCLK_VSB_R
11 SMBDATA_VSB_R



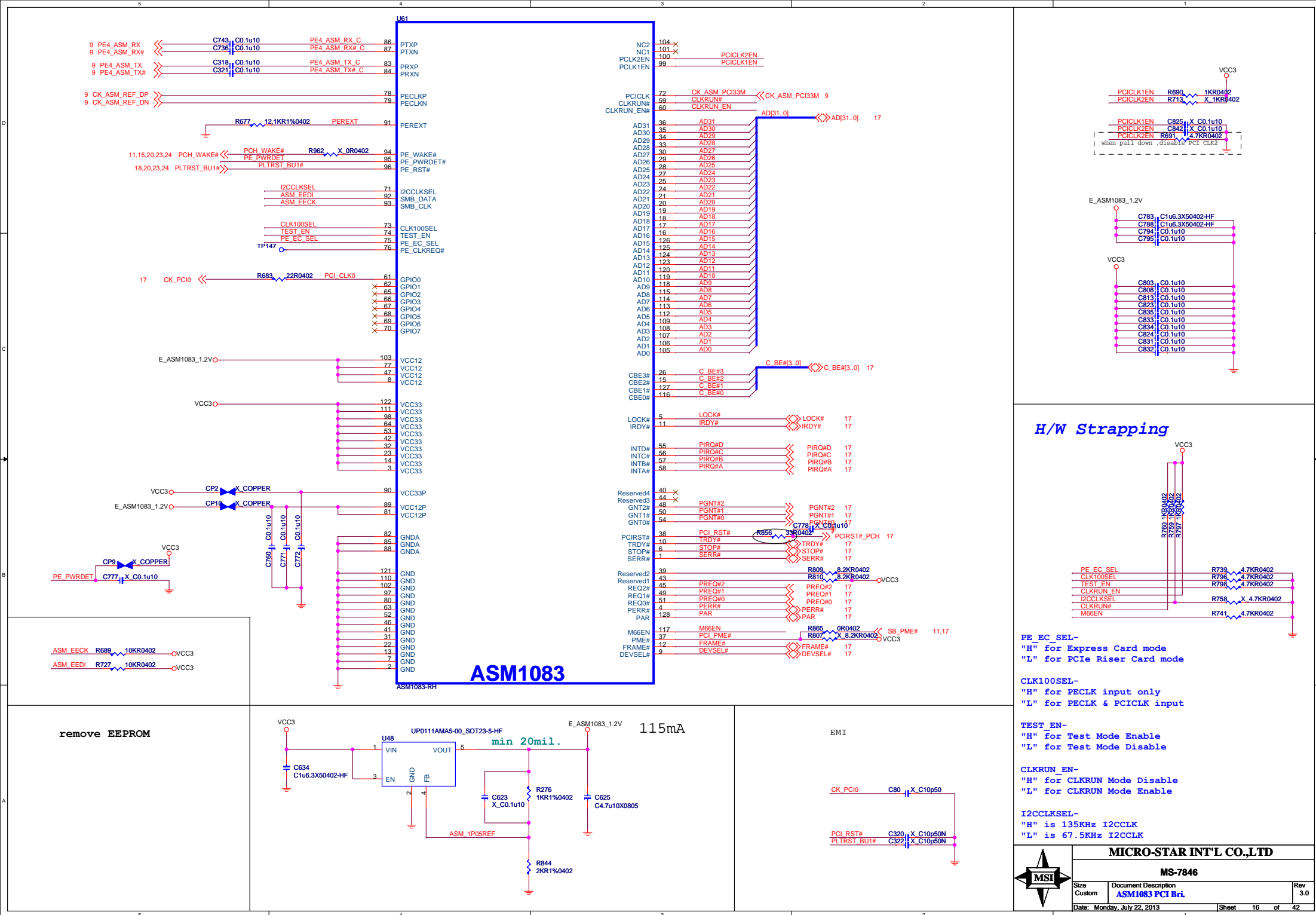
MSI

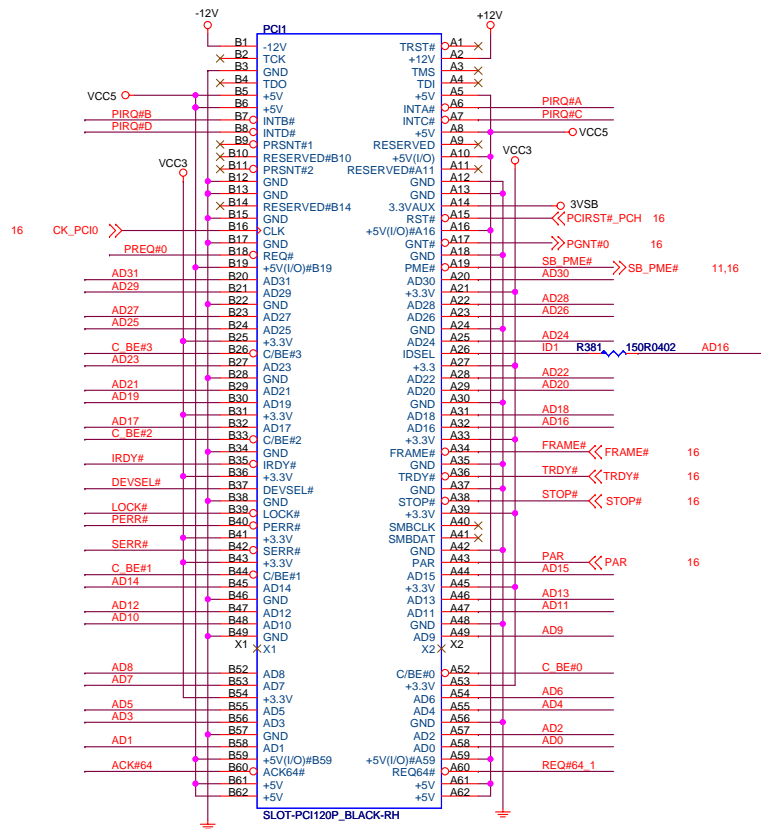
MICRO-STAR INT'L CO.,LTD

MS-7846

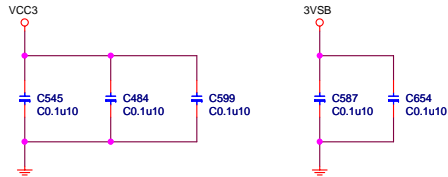
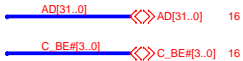
Size	Document Description	Rev
Custom	PCIE1(X1) & PCIE2(X16) Slots	3.0

Date: Monday, July 22, 2013 Sheet 15 of 42

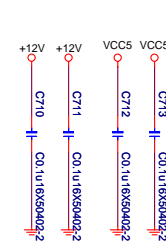
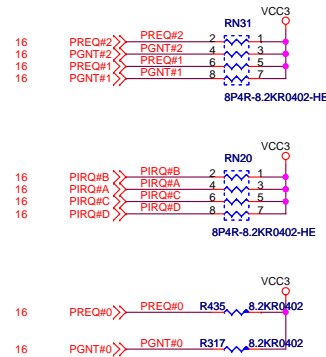
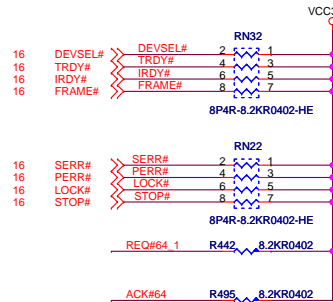




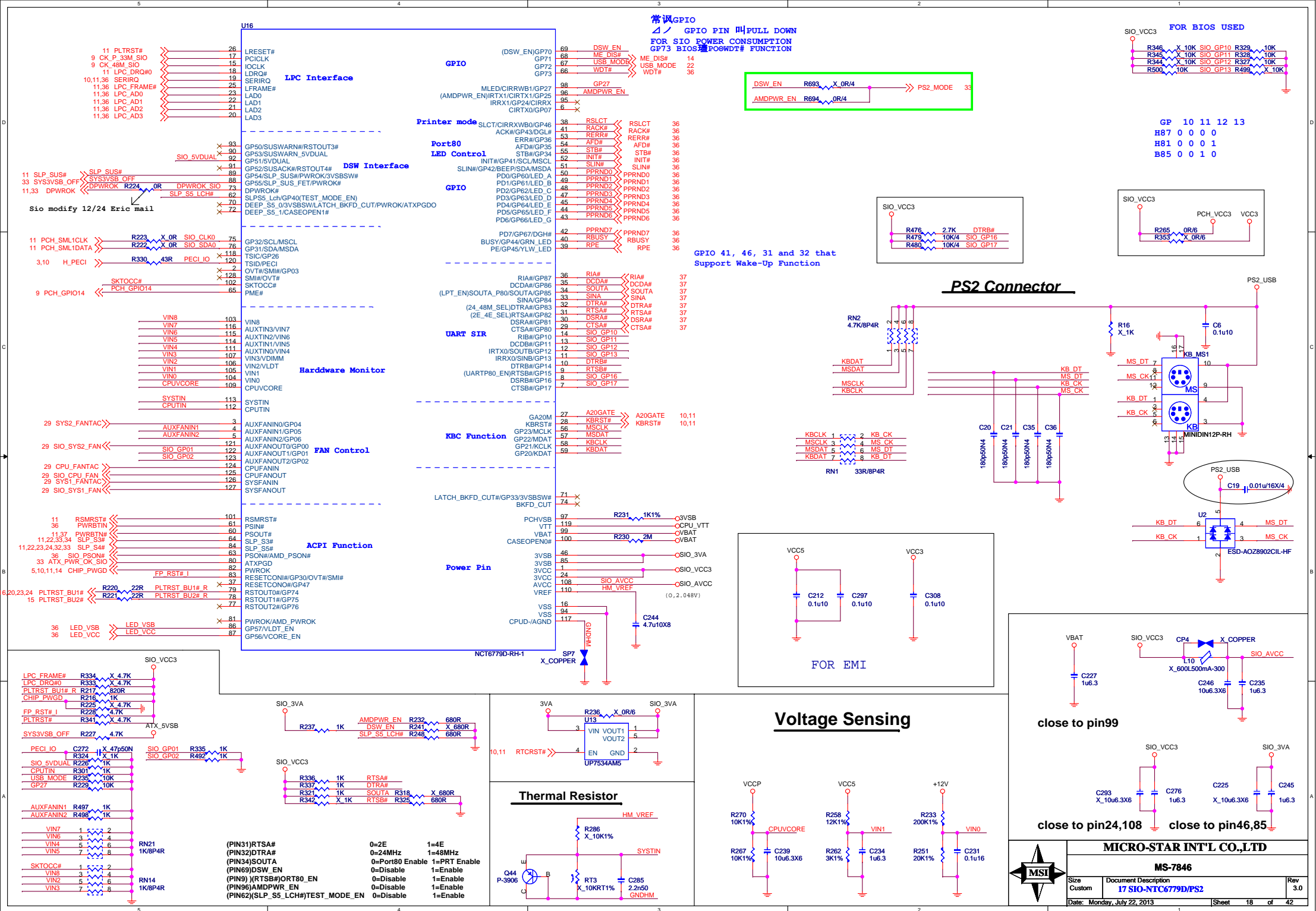
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



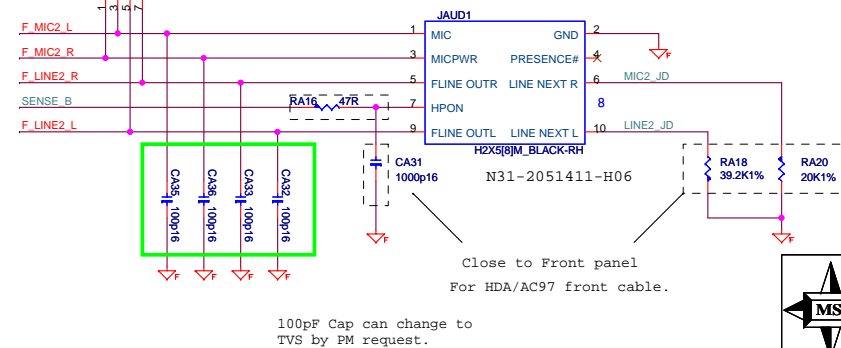
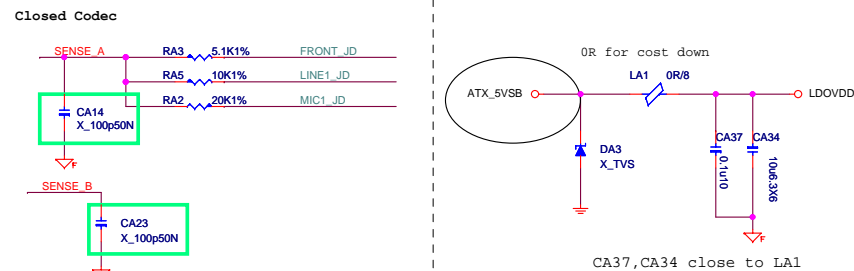
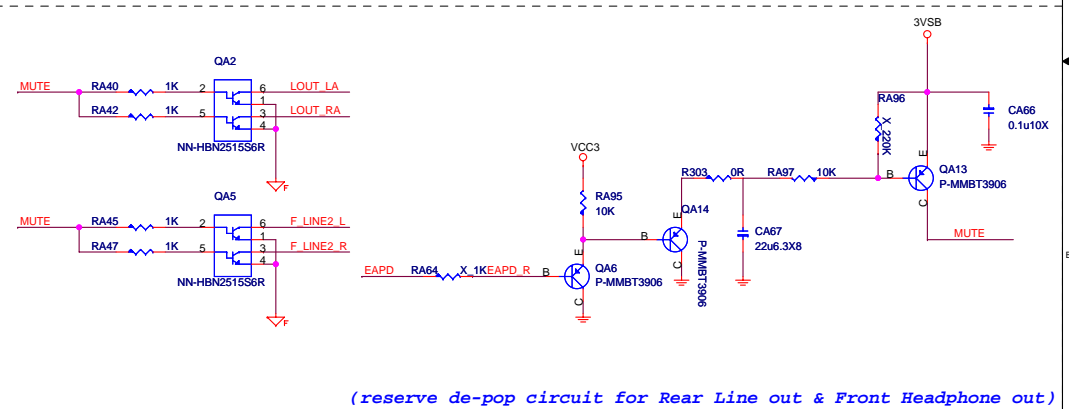
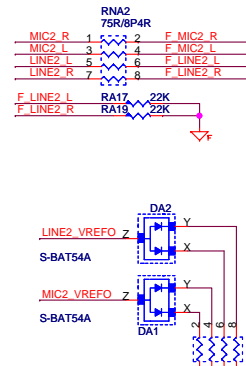
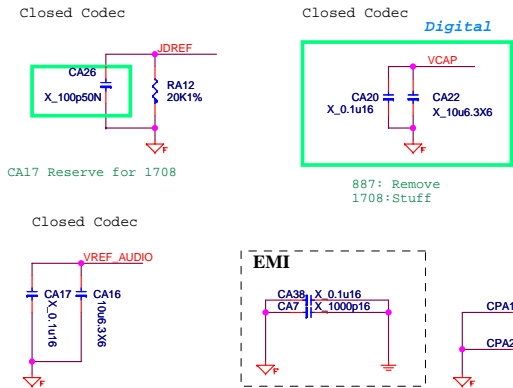
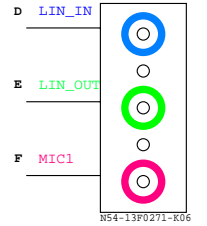
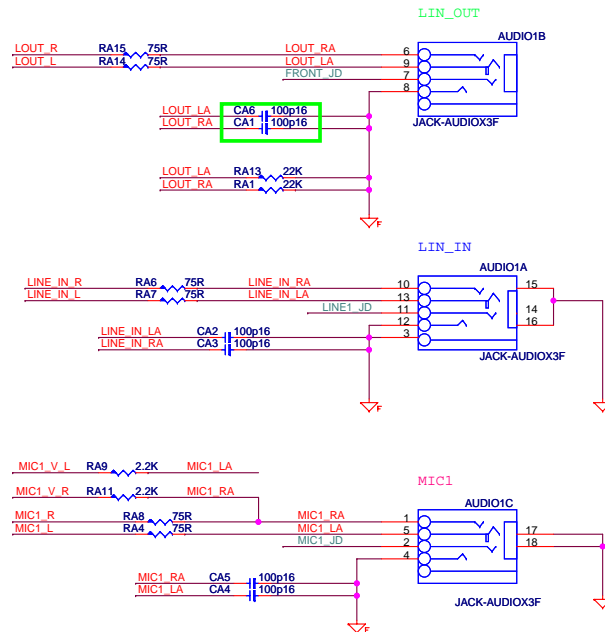
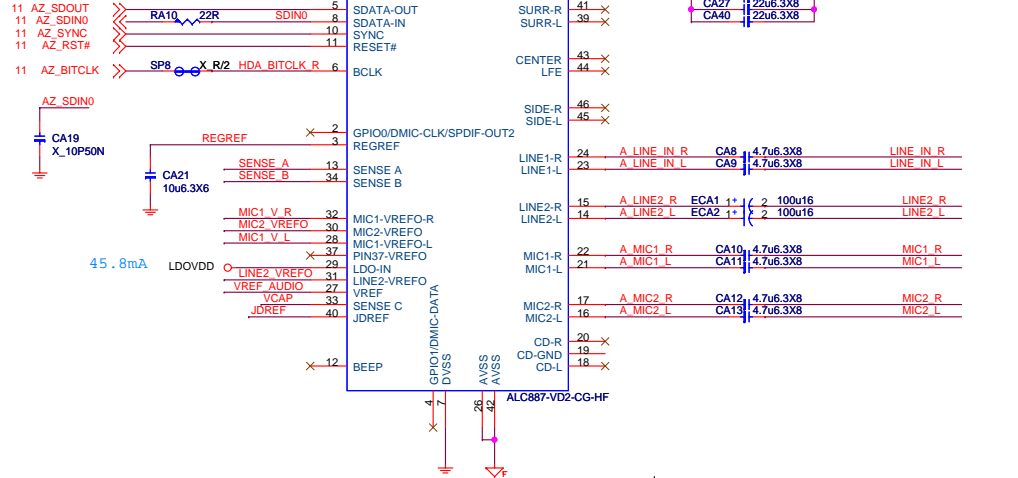
PCI PULL-UP / DOWN RESISTORS



	MICRO-STAR INT'L CO.,LTD		
	MS-7846		
	Size Custom	Document Description PCx1 Slots	Rev 3.0
	Date: Monday, July 22, 2013		Sheet 17 of 42



ALC892/887

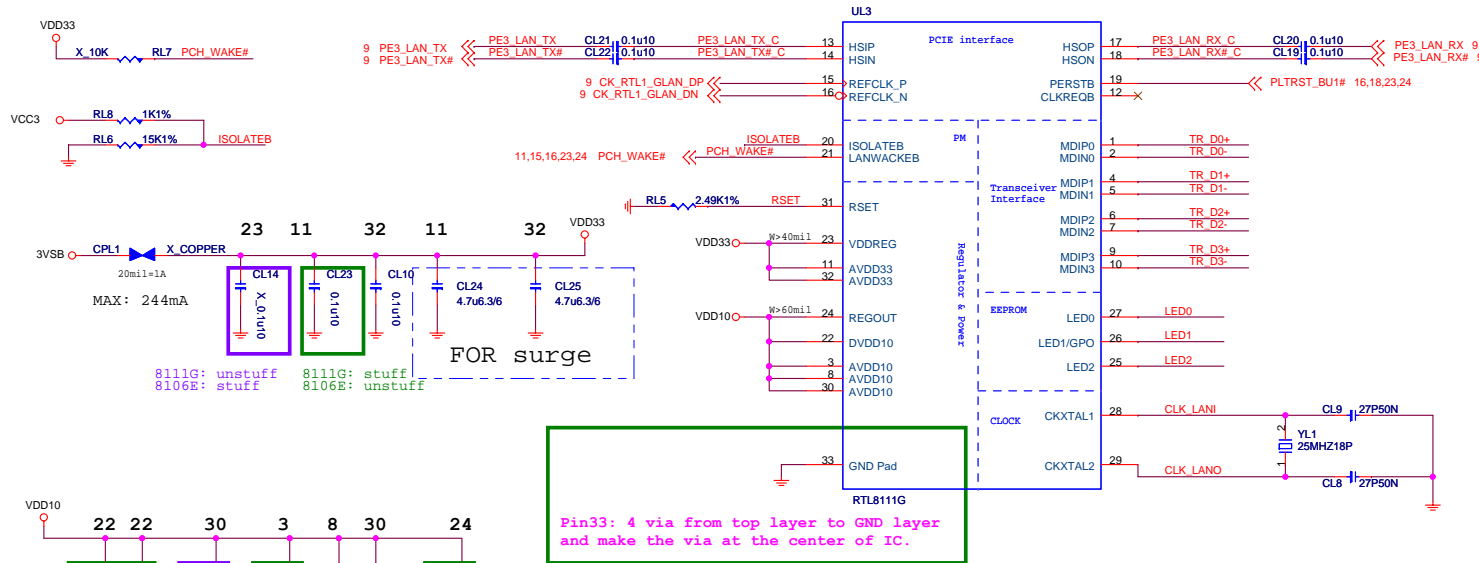


MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size Custom	Document Description Audio Codec ALC892/887		Rev 3.0
Date: Monday, July 22, 2013		Sheet 19 of 42	

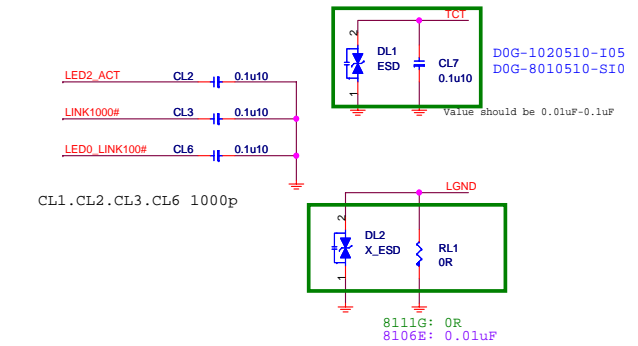
RTL8111G Giga LAN

RTL8106E 10/100M LAN

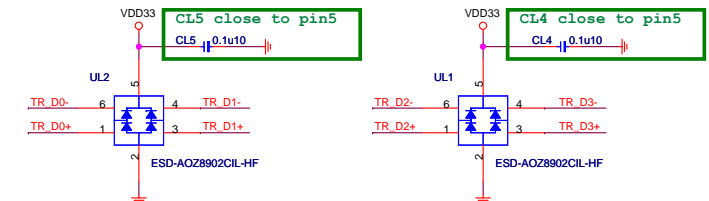
LAN Connector



8111G: Keep RL3 and Remove RL4 for RTL8111G
 8106E: Keep RL4 and Remove RL3 for RTL8106E



Reserve ESD Protect



MSI P/N : D0G-0200529-A68 Vender P/N : AOZ8902CI
 MSI P/N : D0G-0100619-I05 Vender P/N : TVLST2304AD0

8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15



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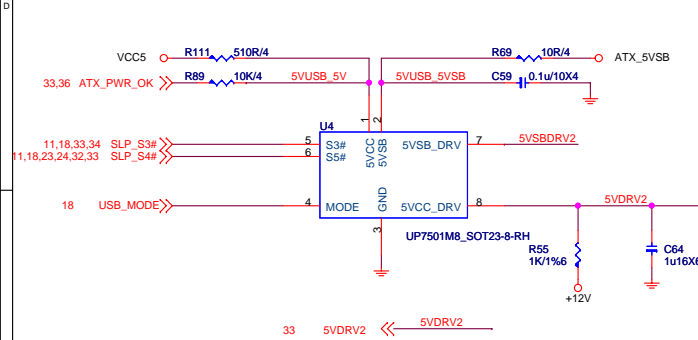
MS-7846

Size	Document Description	Rev
Custom	LAN RTL8111G/8106E	3.0
Date: Monday, July 22, 2013	Sheet 20 of 42	

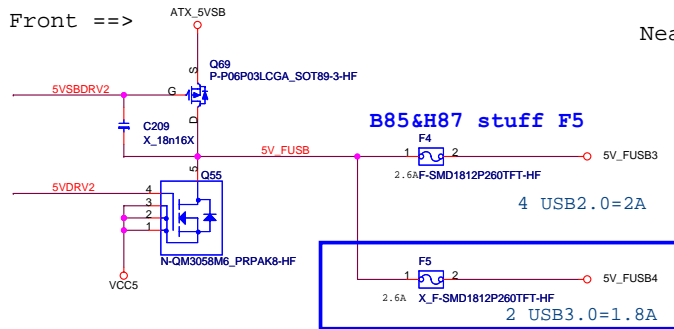
Type A: UP7501+MOS+Fuse

PCH/FCH side: OC# pull high to +3VSB

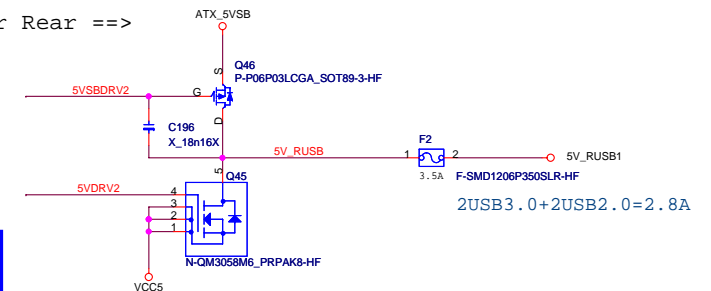
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)
D08-2000200-P16 (Itrip=3.5A; 0.003ohm) MINISMD050



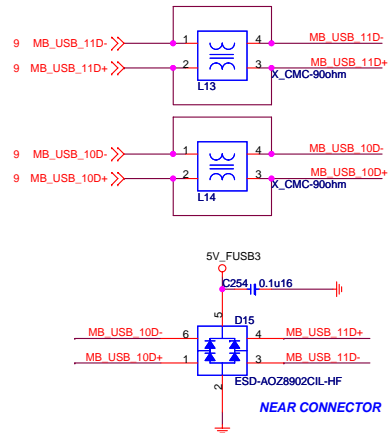
Near Front ==>



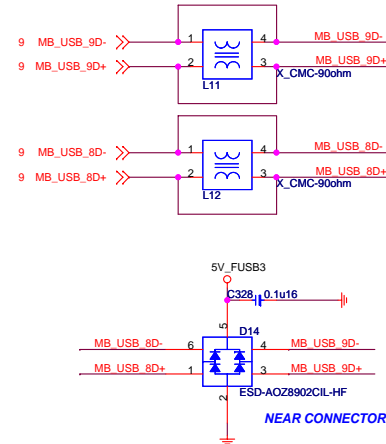
Near Rear ==>



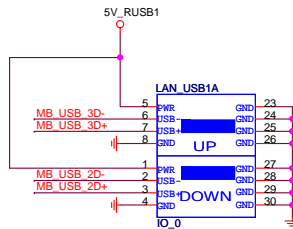
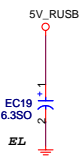
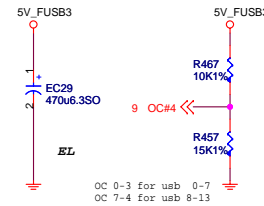
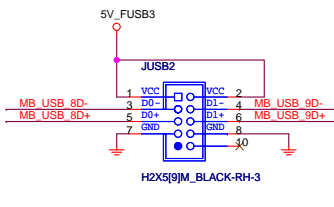
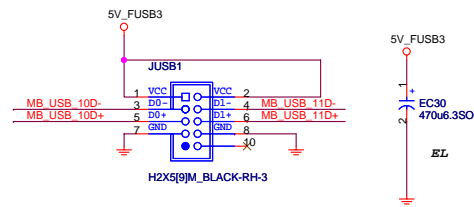
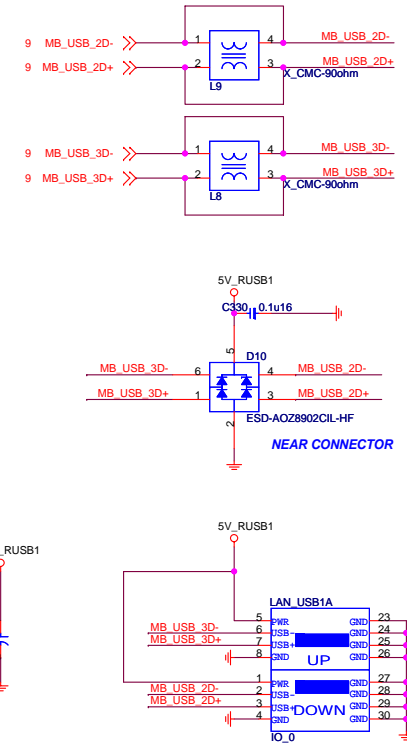
FRONT USB PORT 10,11

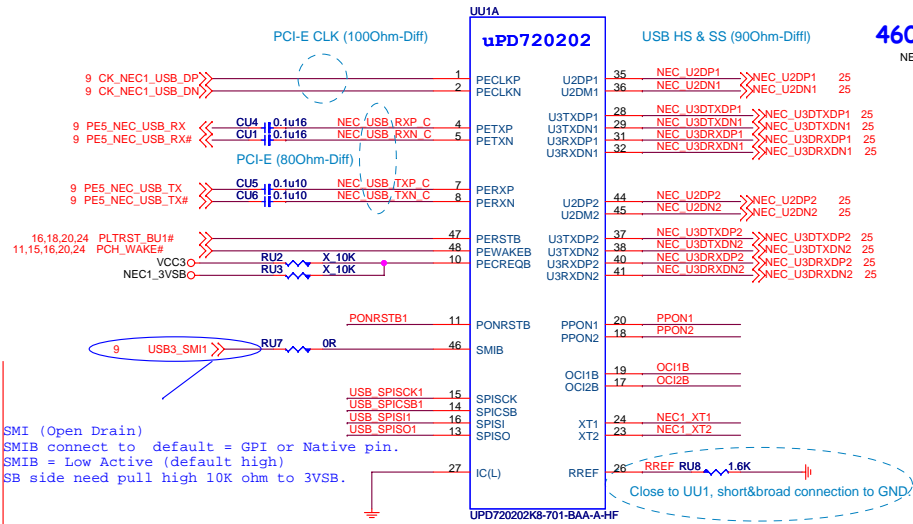


FRONT USB PORT 8,9



REAL USB PORT 12,13

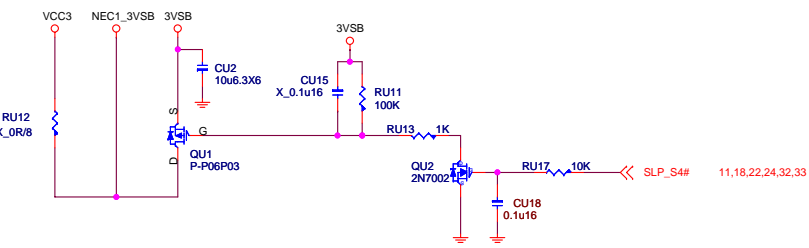




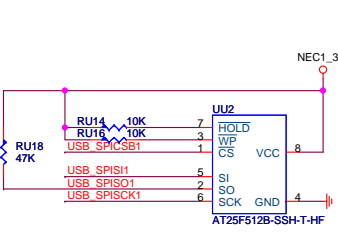
SMI (Open Drain)
SMIB connect to default = GPI or Native pin.
SMIB = Low Active (default high)
SB side need pull high 10K ohm to 3VSB.

P.S. Please don't use SMBALERT# for GPIO.
You may meet auto power on issue with power button shutdown with 4 sec in Cougar Point.
Please use GPI or Native pin for hw default.

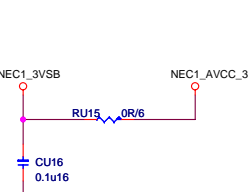
3V_Dual Circuit



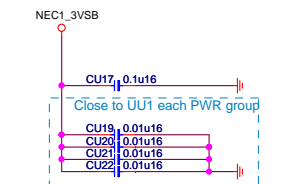
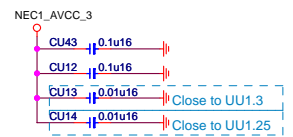
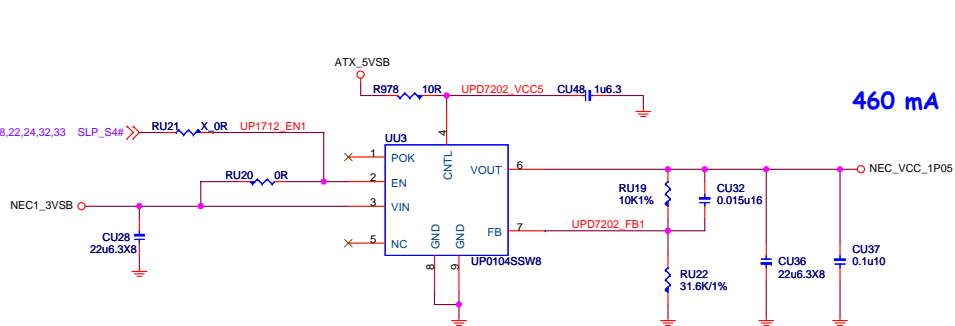
EEPROM



AVCC3 STB Power

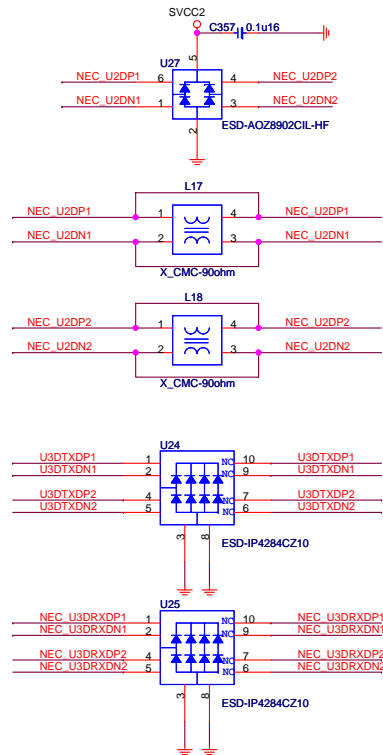


uPD720200 core Power

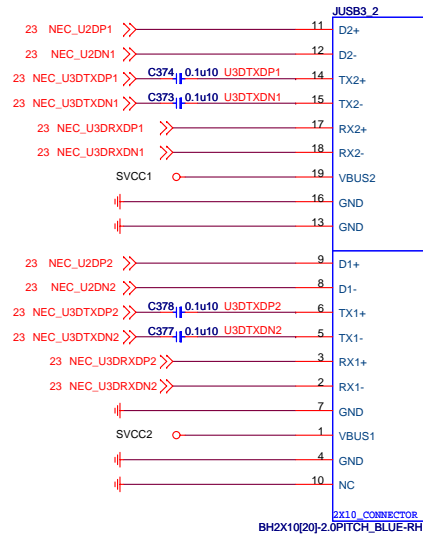


MICRO-STAR INT'L CO.,LTD			
MS-7815			
Size	Document Description	Rev	
Custom	Renesas PD720202 USB3.0 2PORT	3.0	
Date:	Monday, July 22, 2013	Sheet	23 of 42

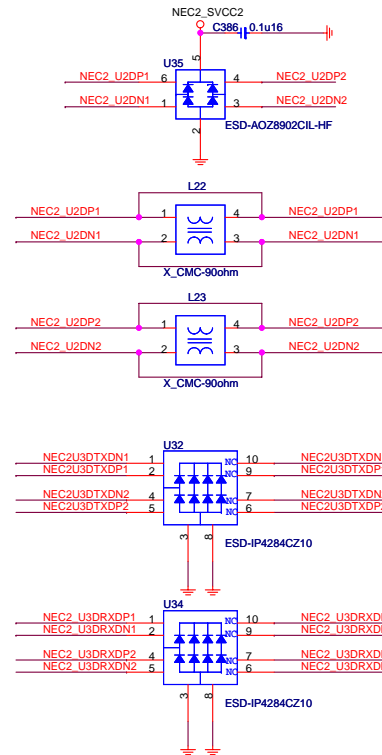
from NEC controller 1
H81 from NEC



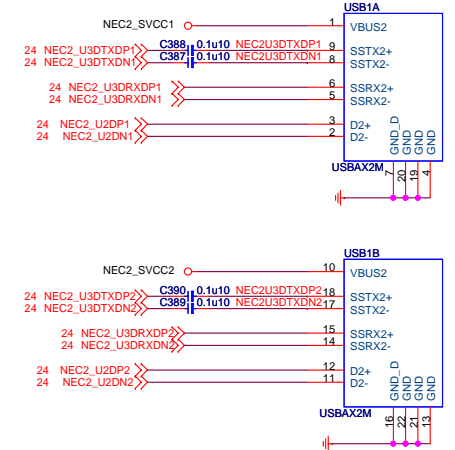
Important--
If USB3.0 signal connect to front pin header,
please must less than 500-700mil is better.
USB3.0 test will fail in factory if you aren't follow this rule.



from NEC controller 2

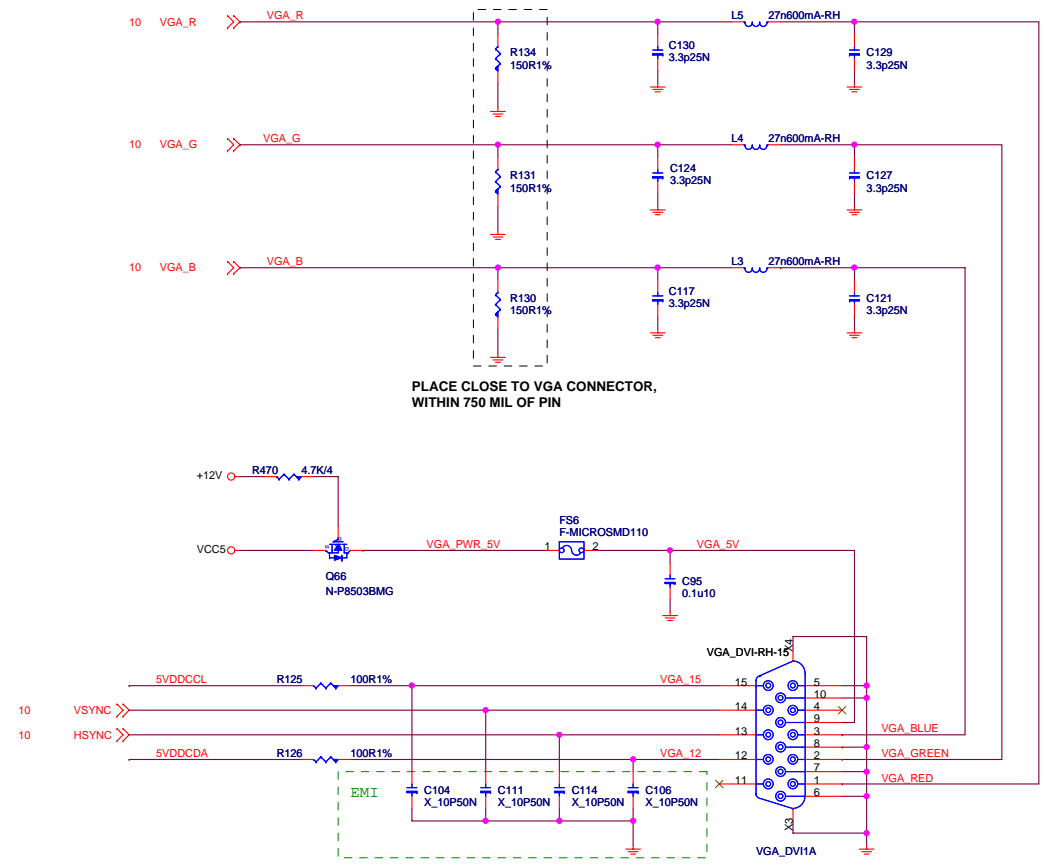
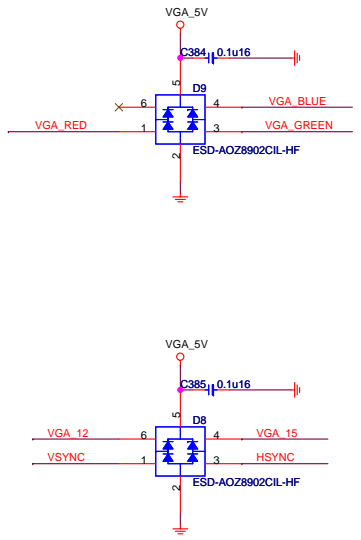
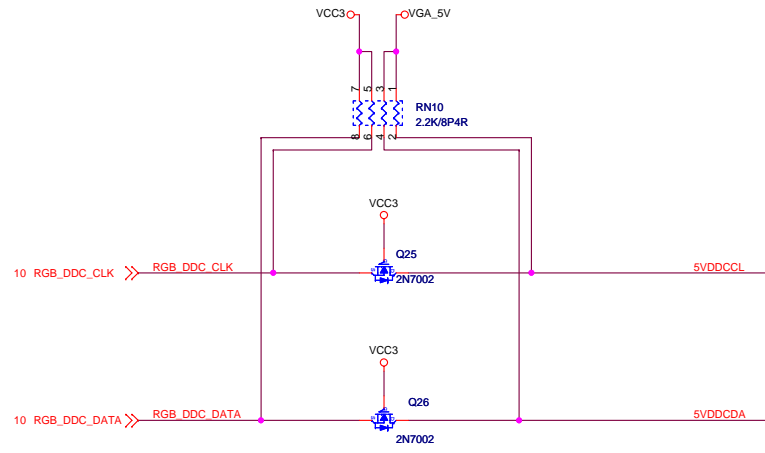


Important--
If USB3.0 signal connect to front pin header,
please must less than 500-700mil is better.
USB3.0 test will fail in factory if you aren't follow this rule.



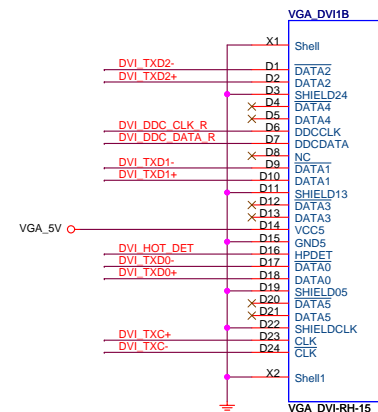
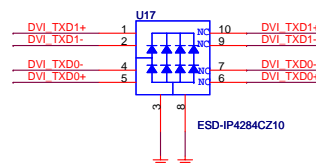
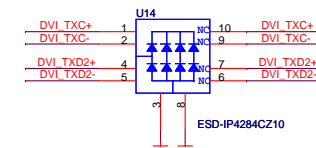
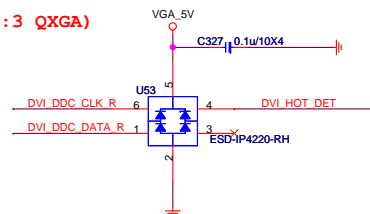
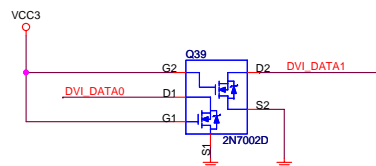
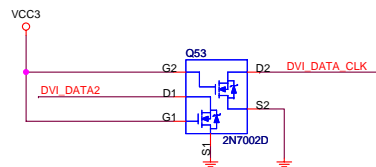
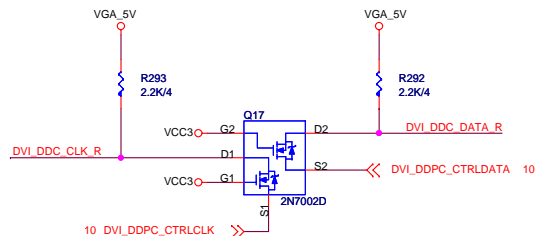
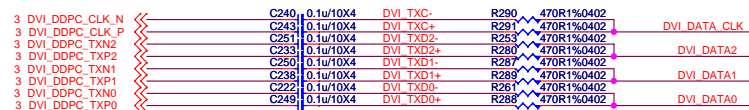
D-Sub

Levelshift

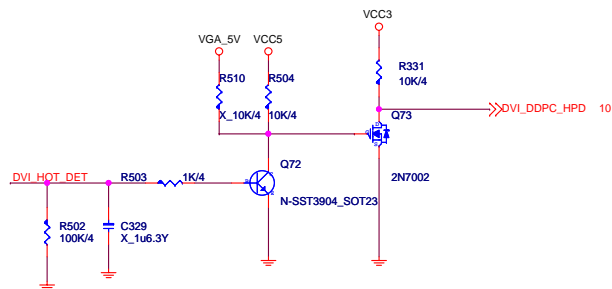


DVI level shifter

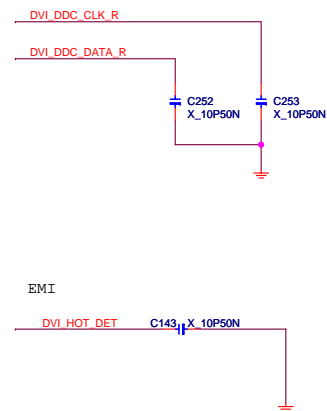
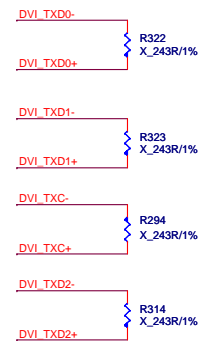
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HPD



For EMI

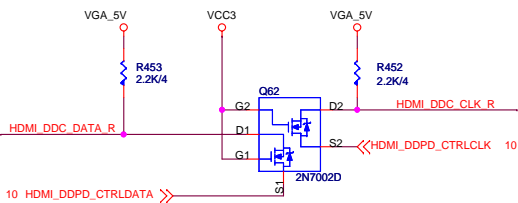
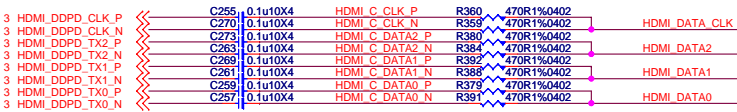


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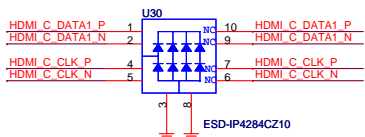
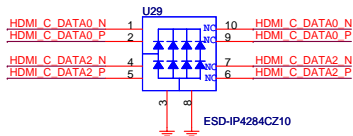
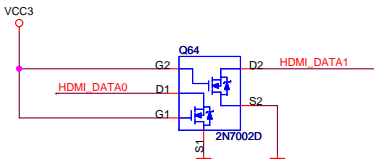
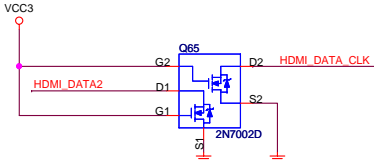
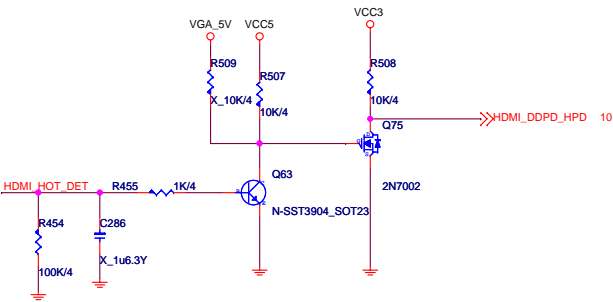
MS-7846

Size	Document Description	Rev
Custom	DVI	3.0
Date: Monday, July 22, 2013	Sheet 27 of 42	

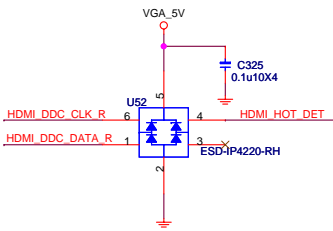
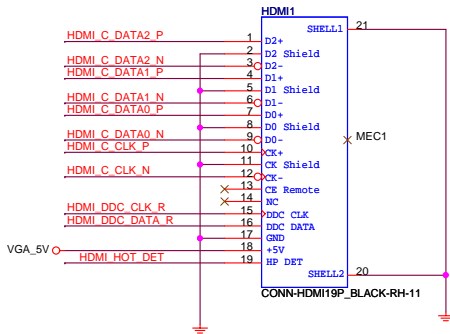
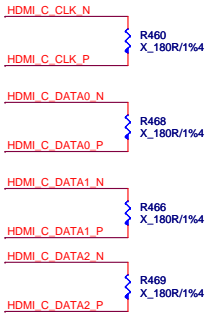
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



HPD



For EMI



EMI



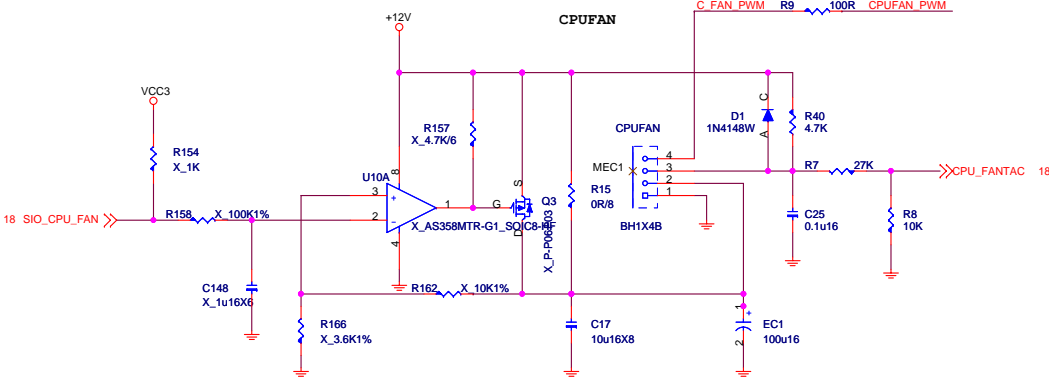
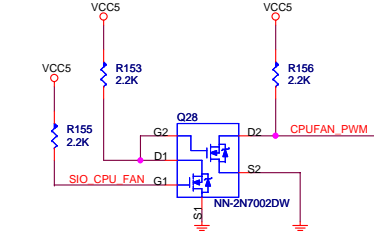
MICRO-STAR INT'L CO.,LTD

MS-7846

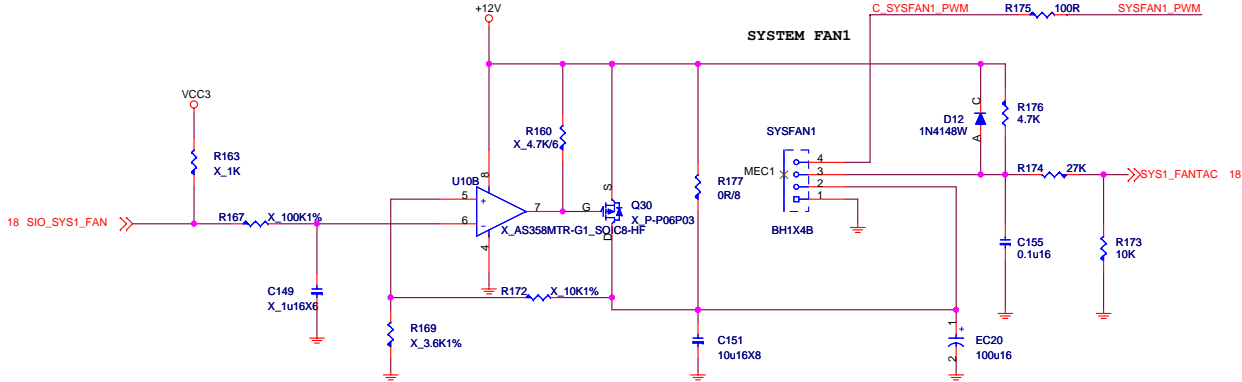
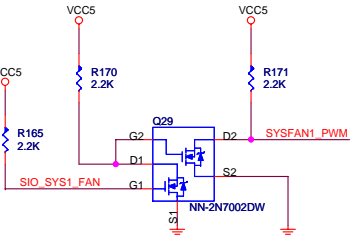
Size	Document Description	Rev
Custom	HDMI	3.0
Date: Monday, July 22, 2013	Sheet 28 of 42	

FAN-COUNTROL CIRCUIT

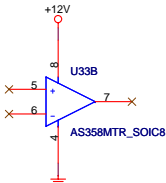
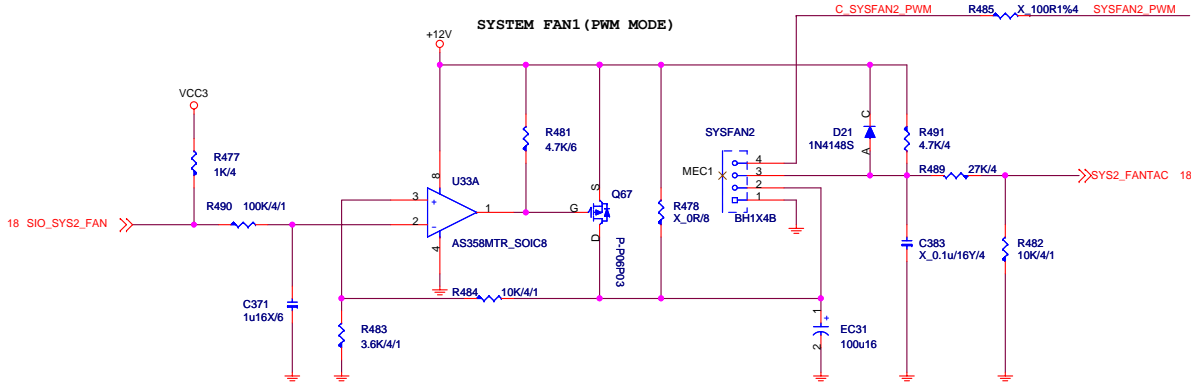
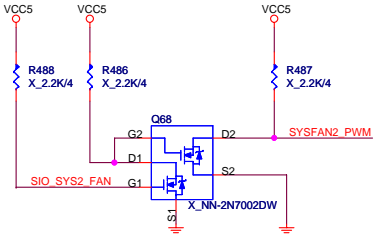
FAN TYPE E



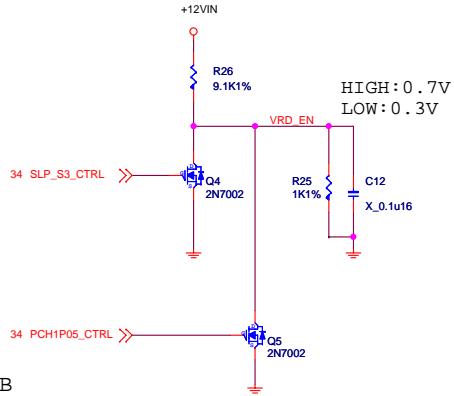
FAN TYPE E



FAN TYPE F



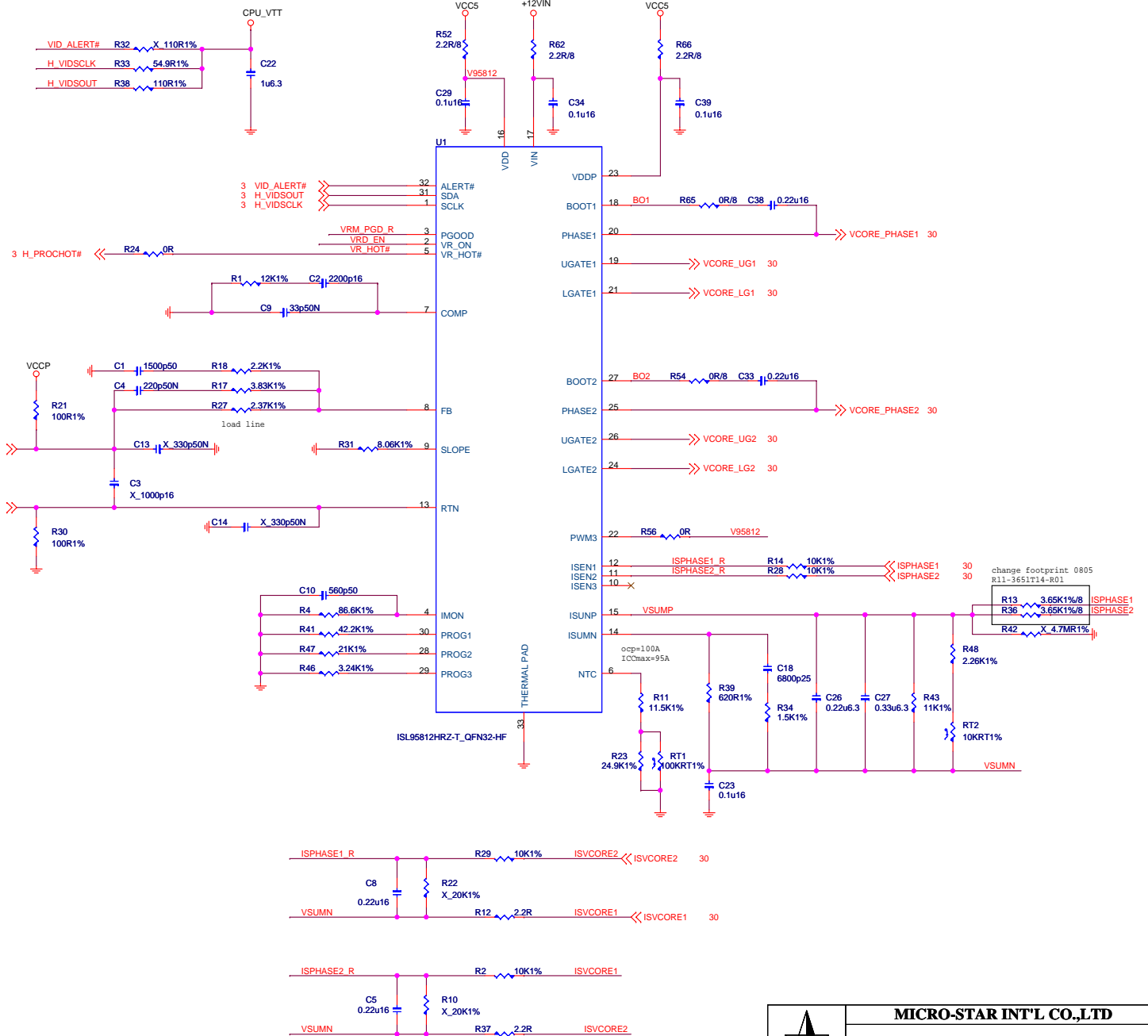
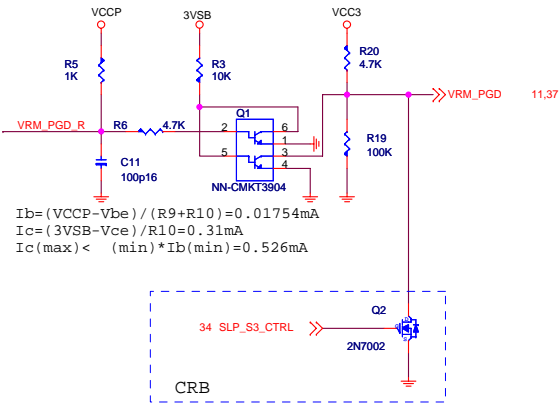
VCORE power on by s3 and 12v



CRB

HIGH:by PCH_1P05V
LOW:by S3

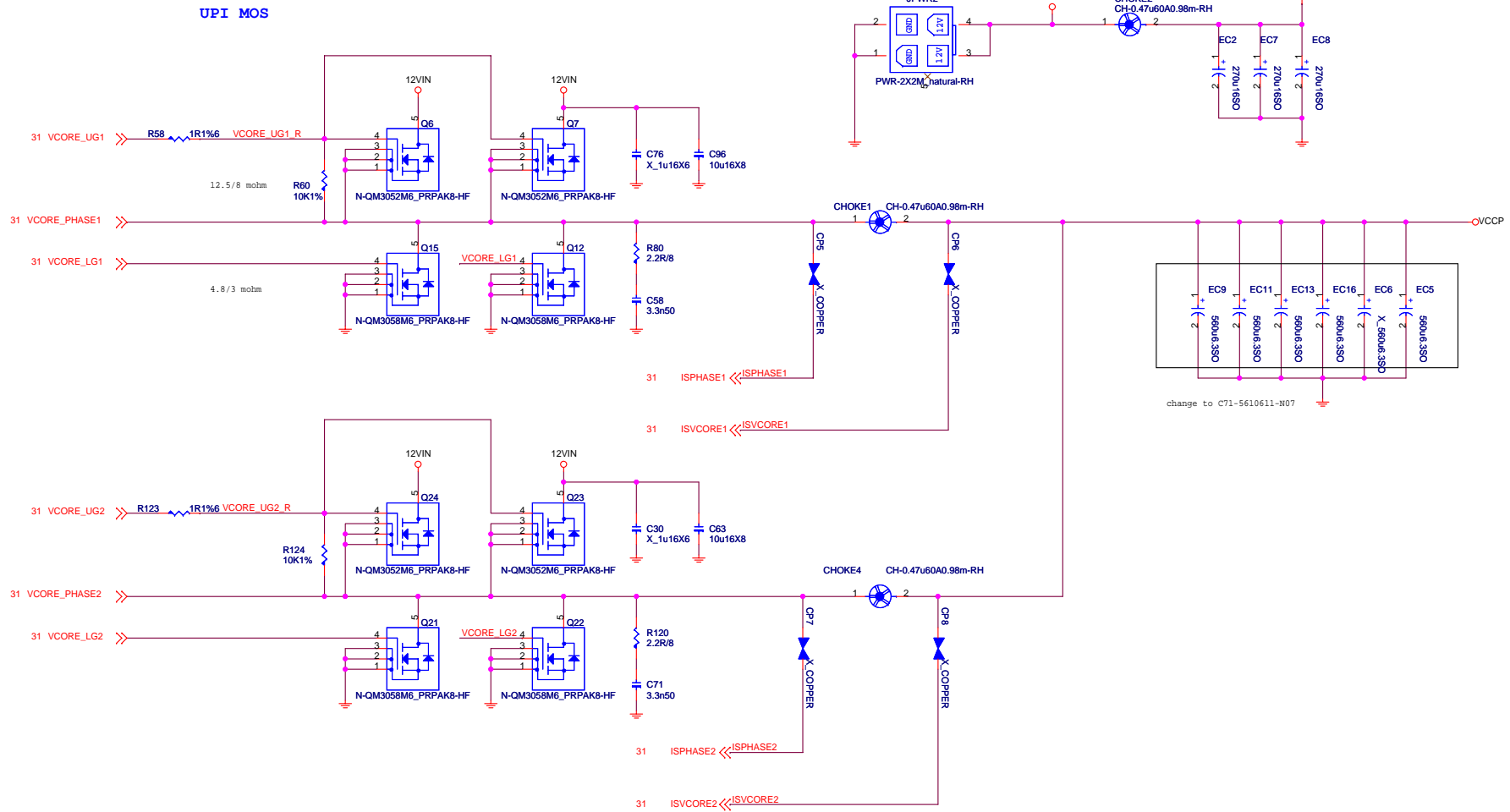
VRMPWRGD LEVEL SHIFT



VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

Irms_input=17.5A



MICRO-STAR INT'L CO.,LTD

MS-7846

Size	Document Description	Rev
Custom	VCCP POWER	3.0
Date: Monday, July 22, 2013	Sheet 31 of 42	

DDR Power:1.5V

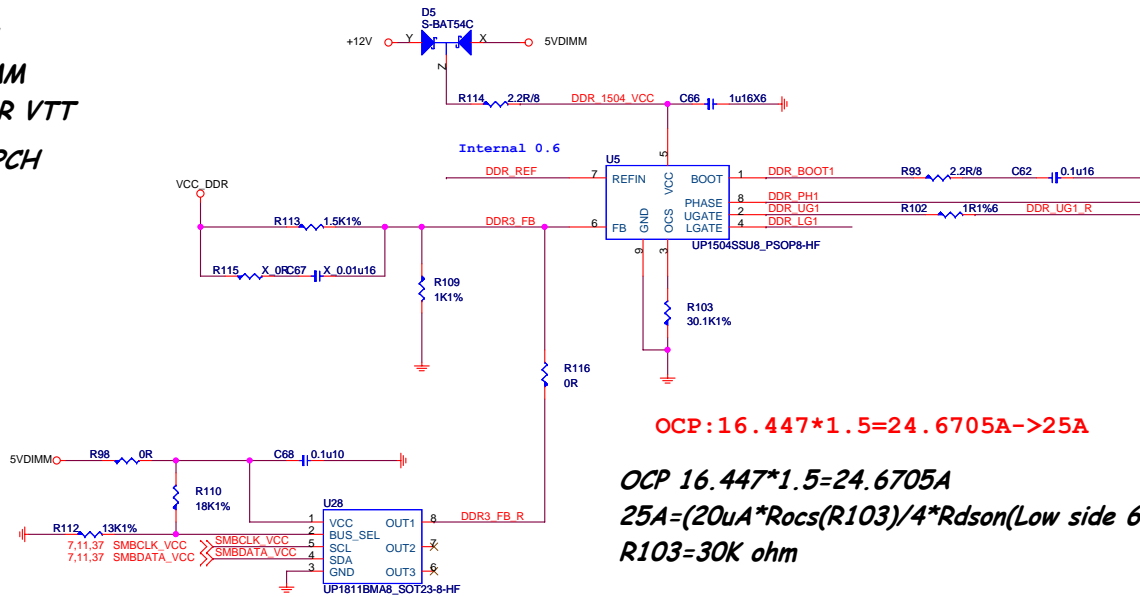
DDR3_1.5V 4.2A+6A+0.5A+5.747=16.447A

4.2A FOR CPU

6A FOR 2DIMM

0.5A FOR DDR VTT

5.747A FOR PCH

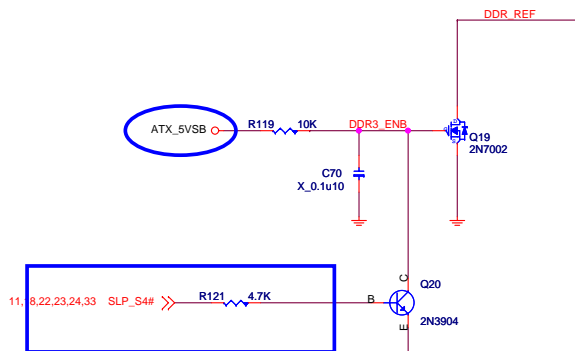
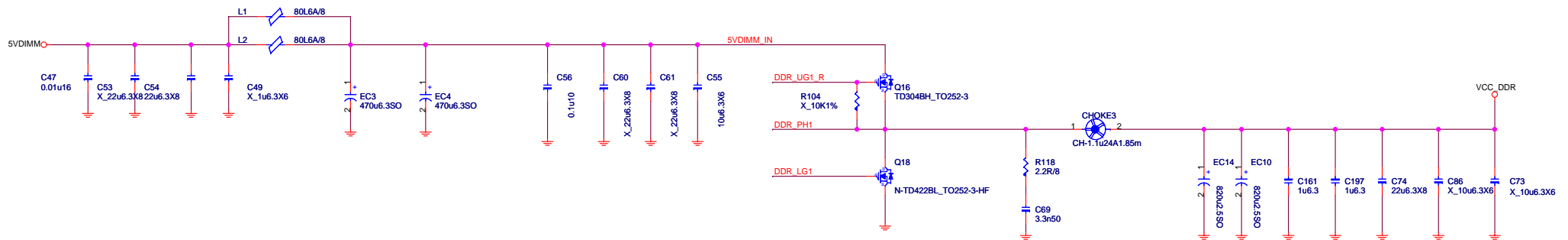


$$OCP: 16.447 \times 1.5 = 24.6705A \rightarrow 25A$$

$$OCP 16.447 \times 1.5 = 24.6705A$$

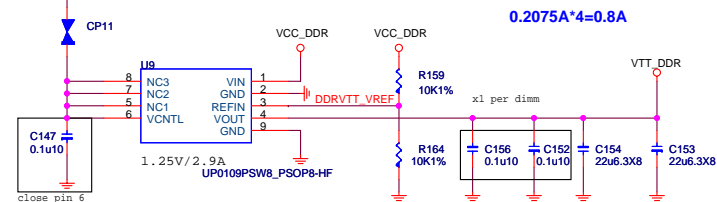
$$25A = (20uA \times R_{ocs}(R103) / 4 \times R_{dson}(\text{Low side } 6mohm))$$

$$R103 = 30K \text{ ohm}$$



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

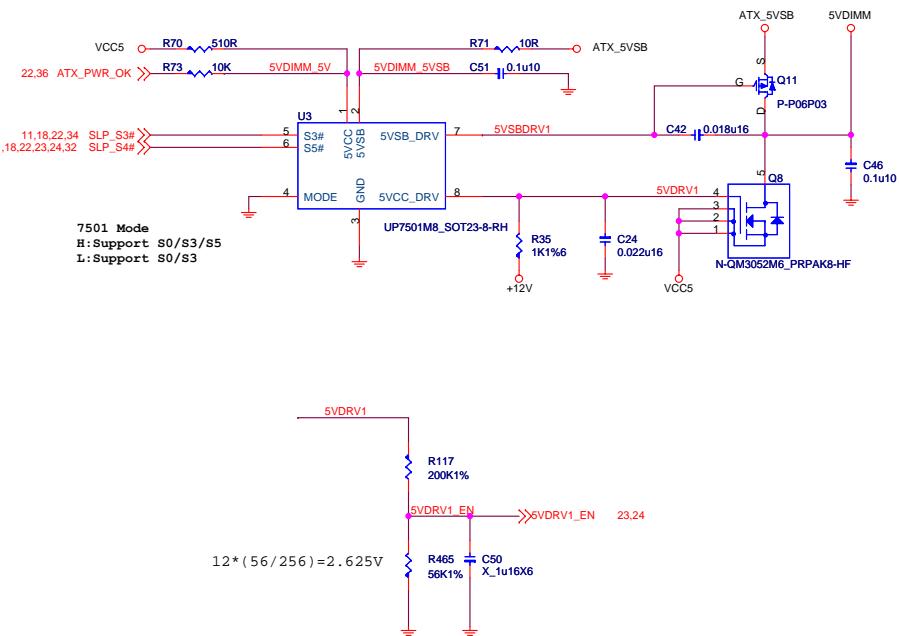


$$0.2075A \times 4 = 0.8A$$

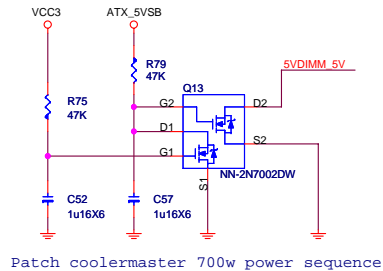
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size Custom	Document Description DDR Power - UP6103 1-Phase	Rev 3.0
Date: Monday, July 22, 2013	Sheet 32	of 42

P.S. Only for meet Intel power down sequence.

5VDIMM FOR DDR

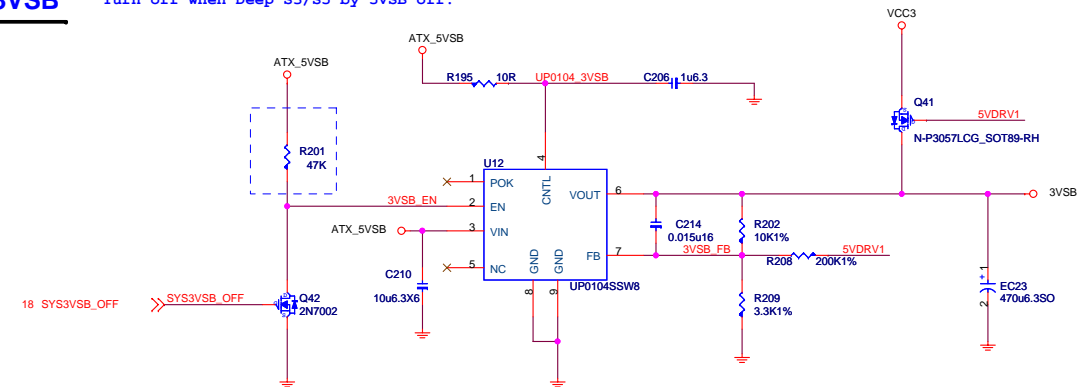


```
For power 700W solution (only for uP7501+uP7506 for 3VSB solution),
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
```



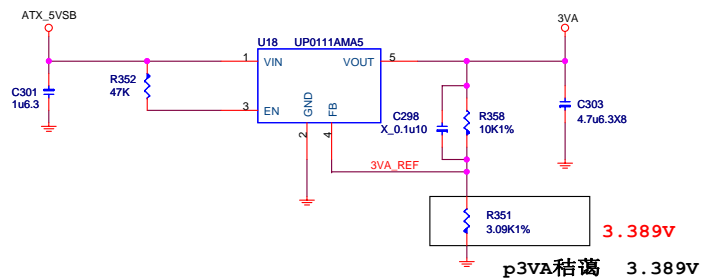
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



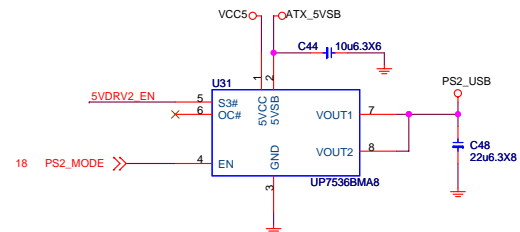
3VA

20mA

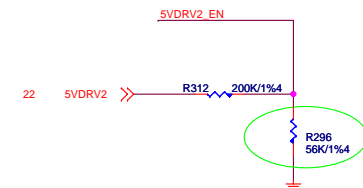


DPWROK惠璫 葦pull down 10k築
杆 紅狠BAT 築琫笛 拜鑼

PS2 Power



USB MODE

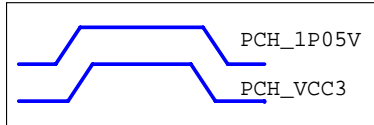
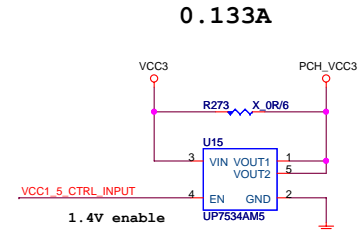
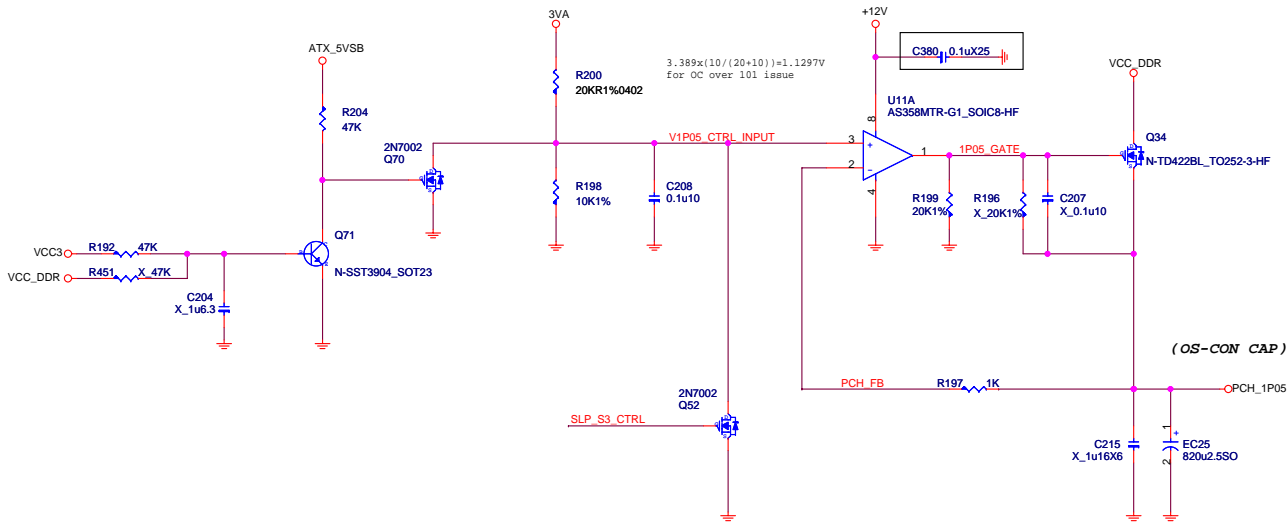


MICRO-STAR INT'L CO.,LTD

MS-7846

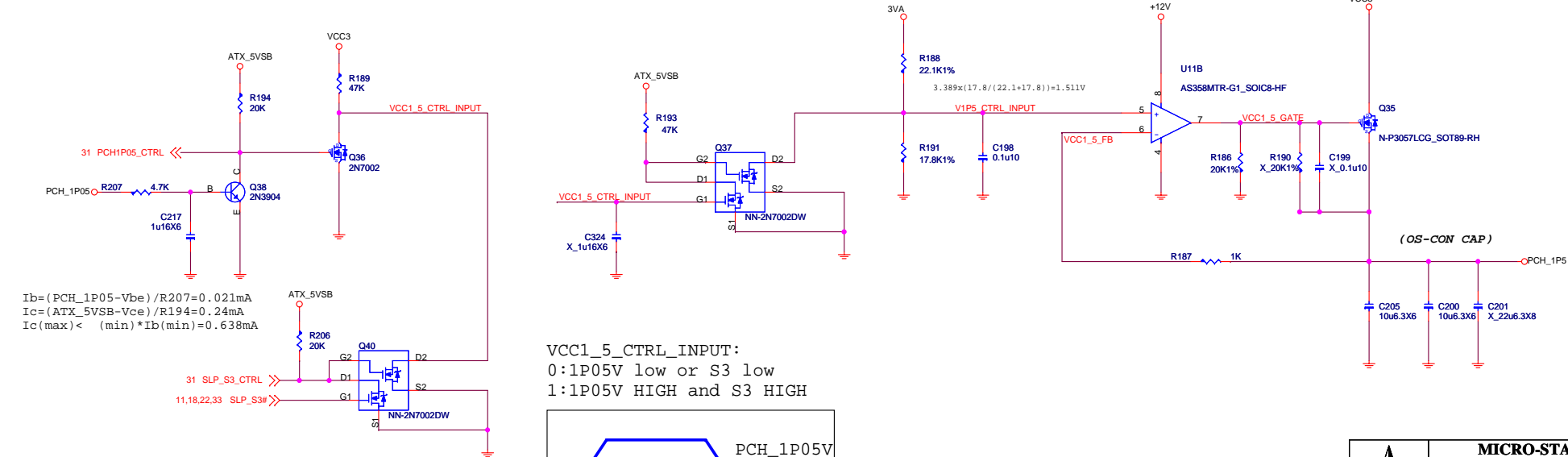
Size Custom	Document Description ACPI controller UPI	Rev 3.0
Date: Monday, July 22, 2013		Sheet 33 of 42

PCH Power:1.05V 5.747A

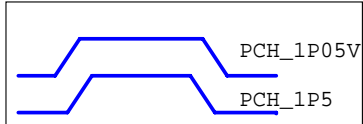


high by VCC3
CRB low by S3

PCH Power:1.5V 0.183A

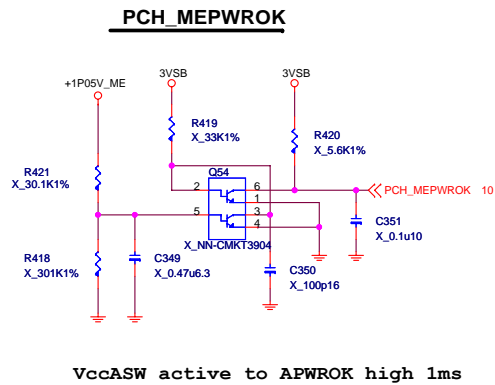
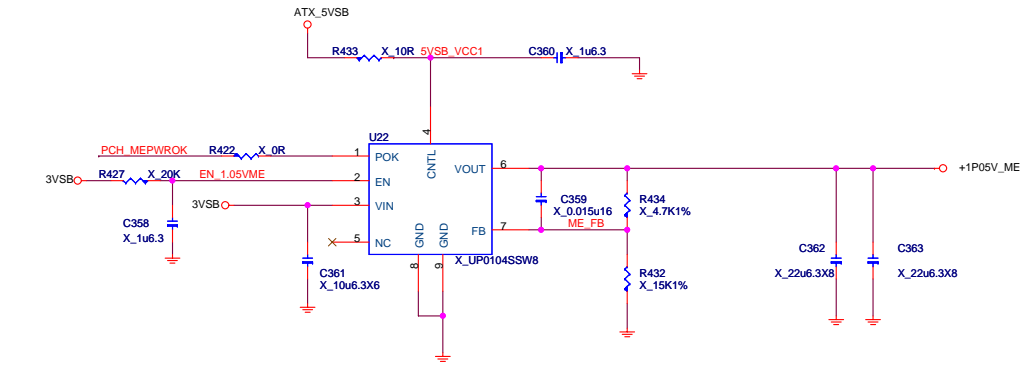
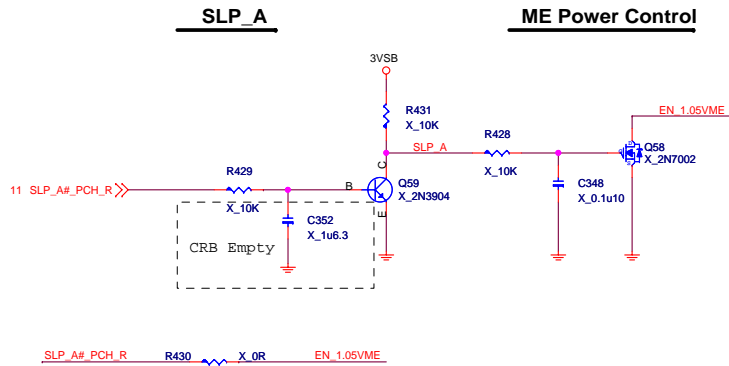


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

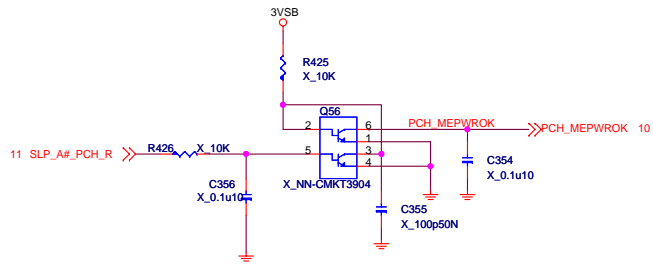


MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size	Document Description	Rev	
Custom	PCH Power - OP+MOS	3.0	
Date:	Monday, July 22, 2013	Sheet	34 of 42

PCH ME Power:1.05V 0.670A

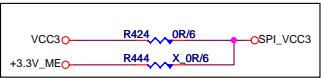


VccASW active to APWROK high 1ms



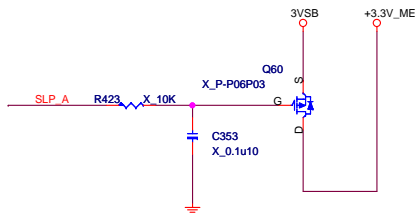
APWROK falling to VccASW falling 40ns

For INTEL ME

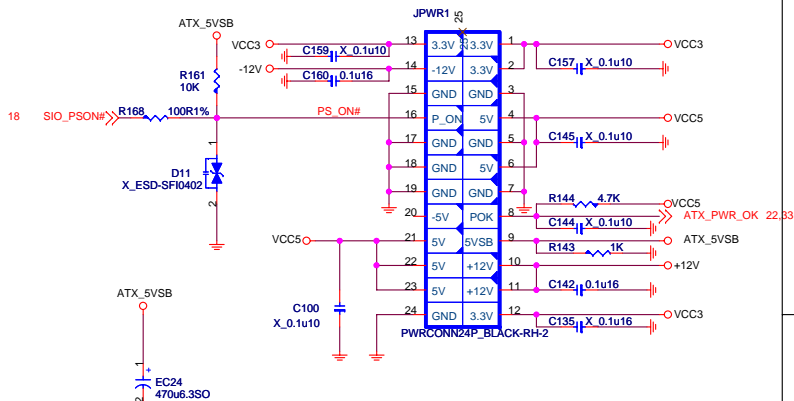


H81 stuff R424
B85 stuff R444

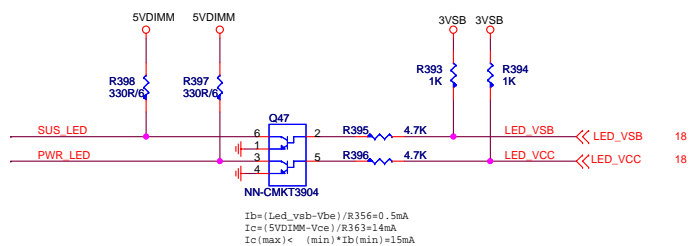
+3.3V_ME



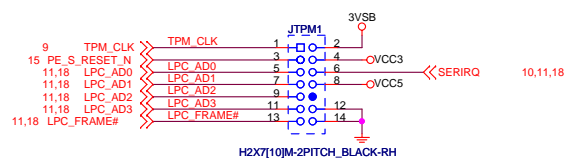
ATX POWER CONNECTOR



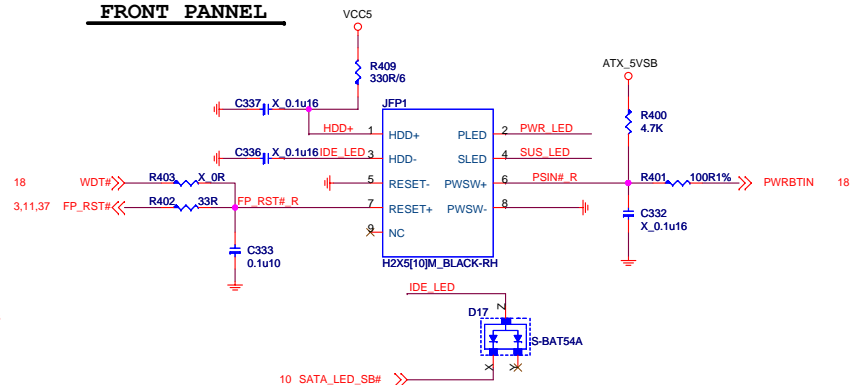
LED (for NV5533)



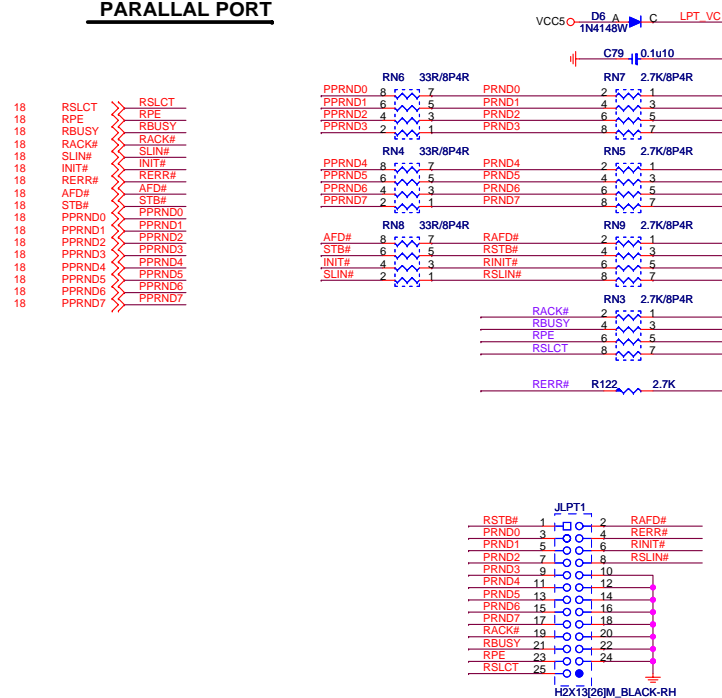
TPM/JLPC



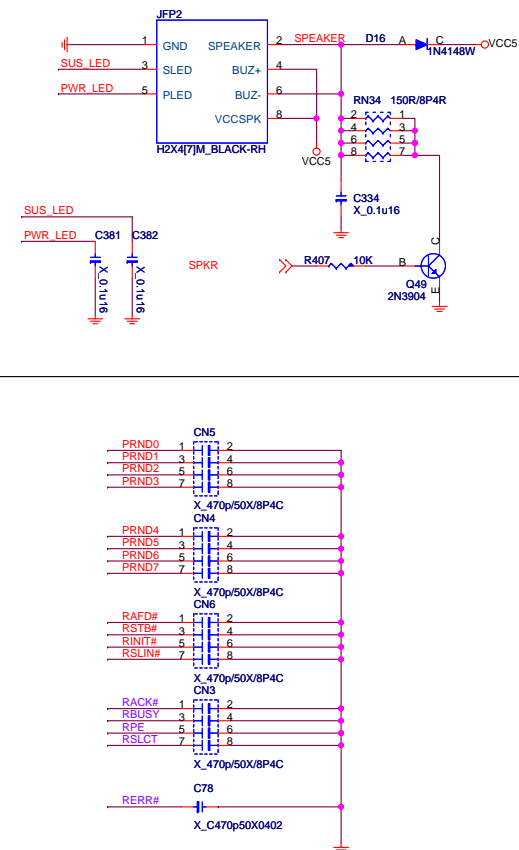
FRONT PANNEL



PARALLAL PORT



Speaker Pin Header

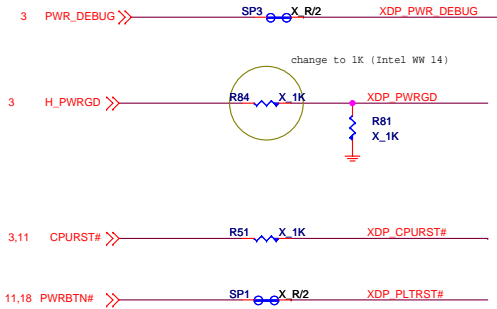
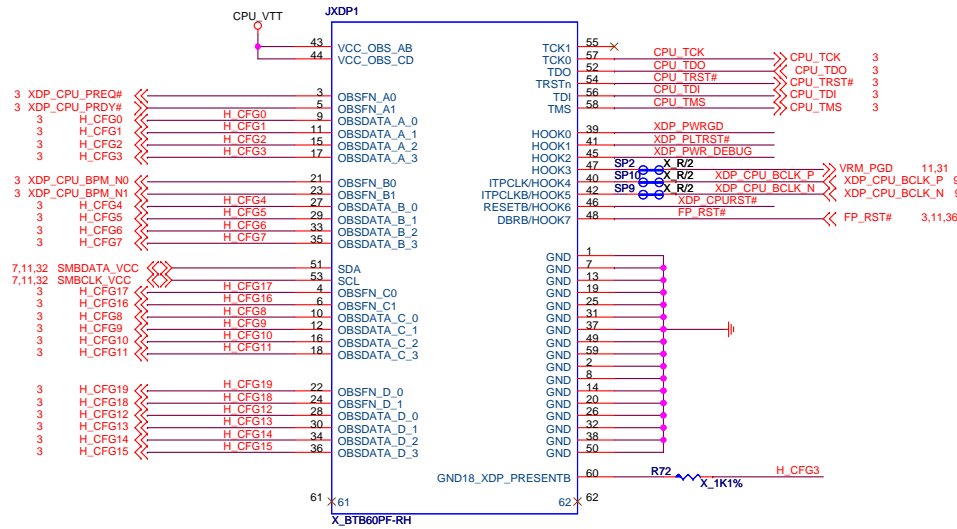


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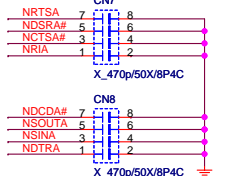
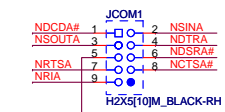
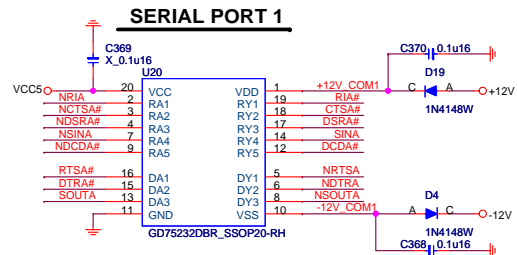
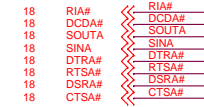
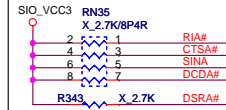
MS-7846

Size Custom	Document Description ATX F_Panel/EMI/TPM	Rev 3.0
Date: Monday, July 22, 2013		Sheet 36 of 42

Reserve debug port 5020



PLACE NEAR XDP CONNECTOR



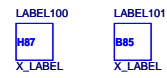
SPI OPT.



CHIPSET OPT.



LABEL OPT.



MK1
G51-M1SPET13-Q13

LA3

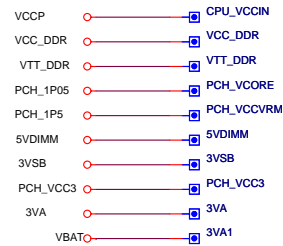
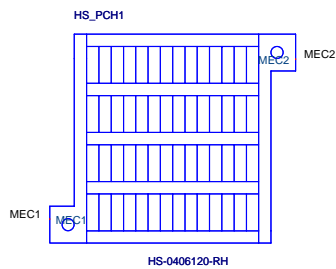


PK0-0784630-G37

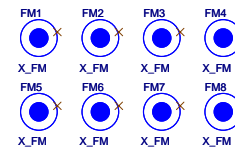
Simulation



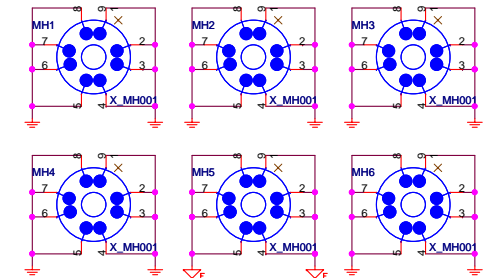
PCH XDP PWRGD/RESET



Optical Fiducial Marks-120



Mounting Holes



MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size Custom	Document Description Manual Parts		Rev 3.0
Date: Monday, July 22, 2013		Sheet 38	of 42



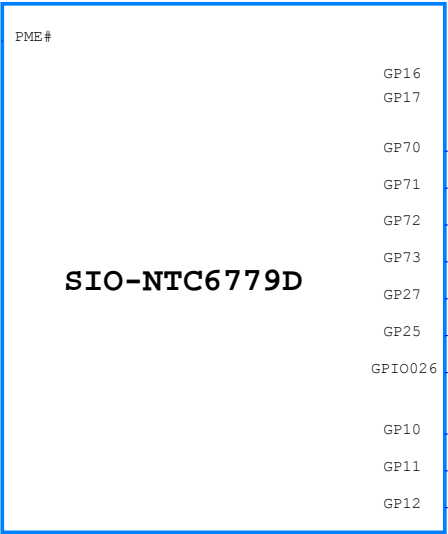
PCIE SLOT

LAN

USB/PS2

EUP Disable
S4/S5 --> support PS2/PCIE Wake
S3 -->support PS2/USB/PCIE Wake

EUP Enable
S4/S5 -->not support any Wake
S3 -->support PS2/USB/PCIE Wake



DSW_EN

ME_DIS#

PS2_MODE

WDT#

TURBO_MODE#

AMDPWR_EN

SIO_GP10

SIO_GP11

SIO_GP12

ME_DIS

OPT BOM
SELECT

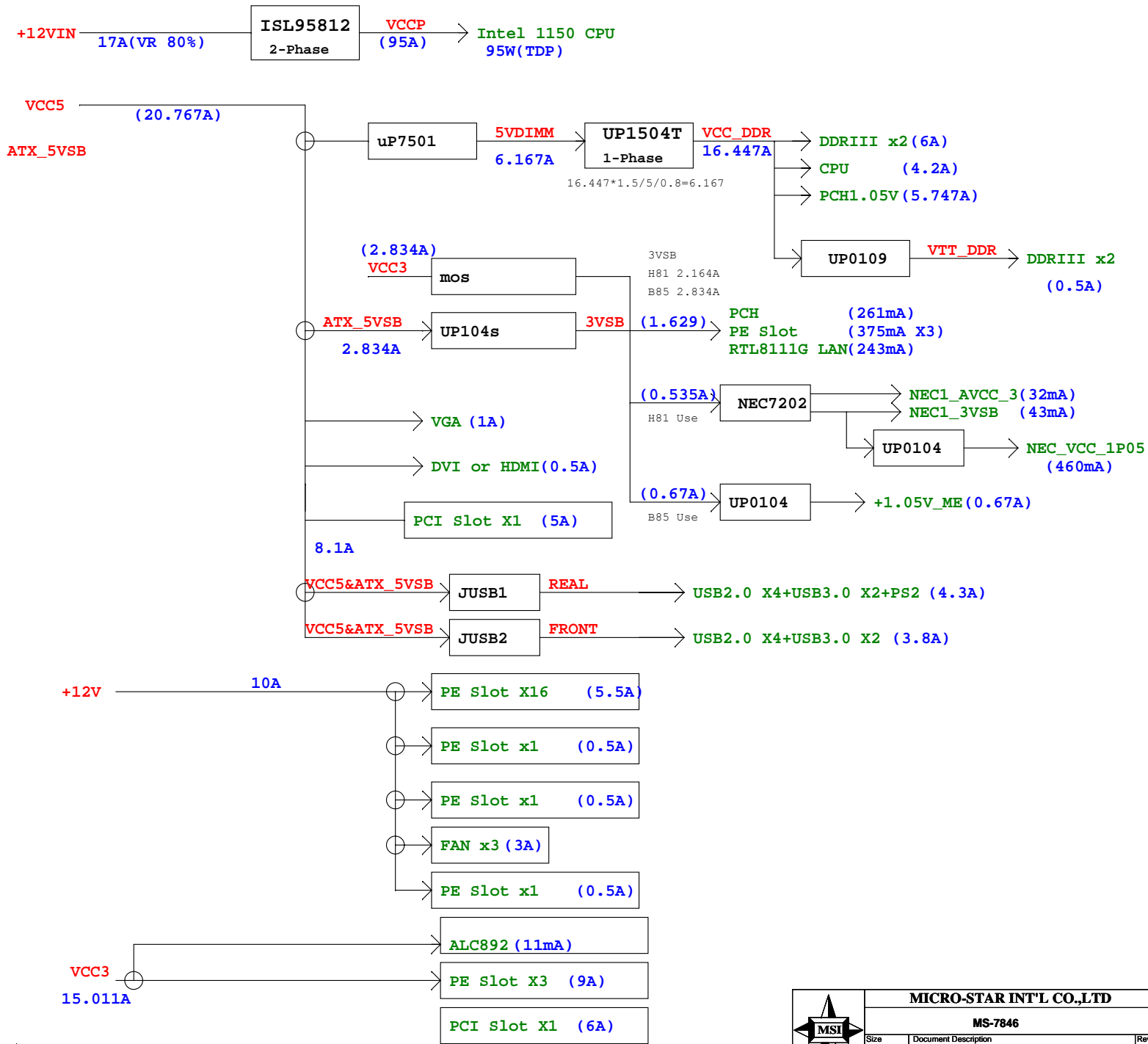


MICRO-STAR INT'L CO.,LTD

MS-7846

Size Custom	Document Description GPIO MAP	Rev 3.0
Date: Monday, July 22, 2013		
Sheet 39 of 42		

+12V	9.5A
+12VIN	17A
ATX_5VSB	9.934A
VCC5	14.767A
VCC3	11.845A



MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size Custom	Document Description POWER MAP	Rev 3.0
Date: Monday, July 22, 2013	Sheet 40 of 42	

(G3)(DS5)

VCCRTC (MB-->PCH) VccRTC active to RTCRST# deassertion: min 9 ms

RTCRST# (MB-->PCH)

ATX 5VSB (PSU-->MB) ATX_5VSB active to DPWROK_CP high min 10 ms

3VA (MB-->PCH)

DPWROK_CP (SIO-->PCH) DPWROK high to SLP_SUS# deassertion min 95ms

SLP_SUS# (PCH-->SIO)

SYS3VSB_OFF (SIO-->MB)

UP0104S 3VSB By 3VSB Ramp up delay

RSMRST# (SIO-->PCH) up: 2.95V down:2.35V

SUSWARN# (PCH-->SIO)

SUSACK# (SIO-->PCH) (SIO delay 250ms as VSB arrives at 2.95V)

PWRBTIN# (SIO to PCH) (CP Internal 16ms debounce)

S5# (By PCH to ???)

S4# (By PCH to SIO)

S3# (By PCH to SIO)

PSON# (as S3) (By SIO to PS) (SIO delay 80ns By SLP_S3#)

12V/5V/3V (By PS to MB) (12/5V -->3V <=20ms)

uP7501 5VDRV1 (By S3 & S4 & 5V) (UP7501 delay 6ms~10ms)

uP7501 5VDIMM (By 5VDRV1)

uP1504 VCC_DDR (By 5V & VCC_DDR to CPU) (By 5VDIMM)

uP0109 VTT_DDR (By 5V & VCC_DDR to CPU)

OP+MOS PCH_1P05 Enable by vcc_ddr

UP0111 PCH_1P5 Enable by PCH_1P05

UP7534 PCH_VCC3 Enable by PCH_1P5

VR_EN (as CPU_SA & 5VSB)

ATX_POK (By PS to SIO 12V/5V/3V Delay 100ms~500ms)

CHIP_PWGD (By ATX_POK & 3V & S3#) (SIO to PCH) (delay 100~200ms)

PCH_MEM_PWRGD (By PCH to CPU) (as CHIP PGD) (CPU: 1ms min)

BCLK (as CHIP_PWGD) (delay 10PCIe CLK 200ns CPUUPWROK)

CPU_PWRGD (by CPU_SA) (PCH to CPU) CPU: 5ms min*2, 650ms max
PSU 500ms + PSU 20ms + PCH t573max + PCH t34

SVID (VR12 to CPU) (By VR_EN Ready (>Vih)) (CPUUPWROK delay500us output SVID)
(VR_EN to SVID , 5ms max)

VIDALERT# (By SVID Ready)

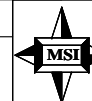
uT501 VCCP

VRM_PG D (VR12 to CLK & PCH) (By VIDALERT Ready)

PLTRST# (PCH to CPU) (By PCH to CPU/SIO) 2-22(CPUUPWROK to PLTRST 100ms max)

CPURST# (PCH to CPU) (By PLTRST#) 2-23

DMI#



MICRO-STAR INT'L CO.,LTD

MS-7846

Size Custom	Document Description Power Sequence	Rev 3.0
Date: Monday, July 22, 2013	Sheet 41 of 42	

7846-2.0

1. 增加 DVI 连接到 HDMI
2. 增加 PCIE slot
3. FAN3 增加 SMART FAN
4. 增加 PCI 增加 ASM1083
5. 增加 COM PORT
6. 增加 马舱 USB port (增加 PS2 增加 USB2.0*2+PS2*1 connector)
7. PCH power Q61 (NN-CMKT3904) 增加 马 Q70 & Q71 (N-SST3904_SOT23)

7846-3.0

base on 7846-2.0 change as follow:

add PCIE -PCI bridge ASM1083 and PCI x1
SMLINK0 DATA/CLK pull up to 499 ohm , SMLINK0 altert#2.2k
change R303 to L21
change c19 to 0.01uf
add DVI /HDMI I2C and detect ESD circuit
change C217 to 1uf
change 1P05V control power to VCC3.3, and change Q71 to N7002
change Q55 Q45 PN follow PWM low side mosfet
change print port to pin head
add two sata port
change PS2+USB2.0 to PS2 and USB2.0
change VGA and DVI to VGA+DVI